Fall 2003

Organic diodes, field -effect transistors, and an inverter circuit by microfabrication techniques

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ORGANIC DIODES, FIELD-EFFECT TRANSISTORS, AND AN INVERTER CIRCUIT BY MICROFABRICATION TECHNIQUES

By

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A Dissertation Presented in Partial Fulfillment of the
Requirement for the Degree of
Doctor of Philosophy in Engineering

COLLEGE OF ENGINEERING AND SCIENCE
LOUISIANA TECH UNIVERSITY

November 2003

ProQuest Information and Learning Company
300 North Zeeb Road
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Date

We hereby recommend that the dissertation prepared under our supervision by GUIRONG LIANG

entitled ORGANIC DIODES, FIELD-EFFECT TRANSISTORS, AND AN INVERTER CIRCUIT BY MICROFABRICATION TECHNIQUES

be accepted in partial fulfillment of the requirements for the Degree of PHD IN ENGINEERING

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ABSTRACT

The objective of this work is to fabricate microelectronic devices and circuits based on organic and polymer materials by microfabrication techniques.

The organic microelectronic device is one of the most promising alternative to traditional inorganic devices due to its varieties of advantages, such as low-cost, large area (e.g. for display), and distinguished mechanical property (insensitive to mechanical deformation). For practical applications, it is necessary to reduce the fabrication cost as well as to improve the device's performance. In this work several fabrication processes have been developed to build organic diodes, field-effect transistors (FETs) and circuits.

Simple spin coating and reactive ion etching (RIE) techniques were used to fabricate the polymer-based Schottky diode and the organic diodes. The Schottky barrier height, breakdown voltage, and rectification ratio of Aluminum/(Poly-3,4-ethylenedioxythiophene/poly-styrenesulfonate) (PEDT/PSS) Schottky diode are about 0.97 eV, 5.5 V, and 1.3×10^4, respectively. The breakdown voltages are about 9 V, and the rectification ratios are in excess of 4.1×10^3 for both Polypyrrole/1,4,5,8-naphthalene-tetracarboxylic-dianhydride (NTCDA) and (PEDT/PSS)/NTCDA diodes.

Due to the excellent electrical conductivity, solution processability, and stability of PEDT/PSS, PEDT/PSS FETs have been investigated and fabricated with the low-cost fabrication processes of spin coating and RIE using an aluminum film as the pattern mask. PEDT/PSS FET with low-resistivity silicon as the gate has a field-effect mobility

as high as 0.8 cm^2/Vs and a threshold voltage of 17 V. All-organic FET has a field-effect mobility of 1.04×10^{-3} cm^2/Vs and a threshold voltage of -13.3 V.

Using thermal oxide and self-assembled silica nanoparticle as the gate dielectrics, pentacene FETs were fabricated and investigated. Temperature-dependence of field effect mobility and threshold voltage was studied in the range of 300 ~ 400 K. Being a low-cost and low-temperature process, layer-by-layer self-assembly technique has been used to form the gate dielectric as an alternative insulator of silicon dioxide to fabricate pentacene FETs. An approach to promote device mobility has also been studied. Moreover, dual-gate pentacene FETs were fabricated as a new device structure with good performance. A simple inverter circuit integrated with a pentacene FET and an ink-jet printed polymer resistor has been fabricated and tested.

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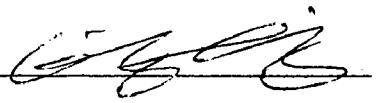
Author 

Date 10-20-2003

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ACKNOWLEDGMENT

I would like to express my sincere gratitude and thanks to my advisor, Dr. Tianhong Cui, who has instructed me in the scientific method and honest attitude, and co-advisor, Dr. Kody Varahramyan, for his discussion and support. Their invaluable advice, continuous guidance, encouragement, and assistance are necessary for completion of this dissertation. Special acknowledgements are extended to Dr. Frank Ji, Dr. Cheng Luo, and Mr. Ji Fang for their advice and serving as advisory committee members of this dissertation.

The author would like to thank the staff at Institute for Micromanufacturing for their help and support on the process. Much gratitude is extended to Jingshi Shi, Mo Zhu, and Yi Liu for their valuable discussion, support, and contributions.

Thank God for His grace and love. Finally, I dedicate this dissertation to my parents whose love and encouragement accompanied me through this research.

CHAPTER ONE

INTRODUCTION

1.1 Conducting Polymer and Organic Microelectronics

For the past several decades, polymers have increasingly been used as the insulators in the electronic devices and integrated circuits. The electrical conductivity in these polymers was observed to be very low, less than 10^{-5} S/cm. However, in 1977, the first highly conducting polymer, more commonly known as "synthetic metal," chemically and electrochemically doped polyacetylene was reported [1]. This opened an entire new field, and for the discovery and development of conducting polymers, the Nobel Prize in Chemistry was awarded to Alan J. Heeger, Alan G. MacDiarmid and Hideki Shirakawa in the year 2000 [2]. Although initially these doped conducting polymers were unstable in air and difficult to process, new generations of conducting polymers are greatly improved to be air-stable and easily processable from a variety of solvents. Up to now, as shown in Figure 1-1, the electrical conductivities range from those typical for insulators ($<10^{-10}$ S/cm), to those typical for semiconductor ($\sim10^{-4}$ S/cm), to those ($>10^{4}$ S/cm) [3].

The discovery of conducting polymers not only challenged the scientists to gain insight of the conducting mechanism, but also attracted the interest of industry for novel electronic devices and commercial products with low fabrication cost. In the area of low end and high-volume microelectronics, the excellent performance of silicon technology

may not be required as it results in high production costs. On the other hand, mechanical flexibility is often necessary, as this would allow the integrated circuits to be twisted, bent or rolled without any effect on the electrical characteristics of the device. Furthermore, it triggered the research and development of alternative processing technologies to the standard silicon based semiconductor technology.

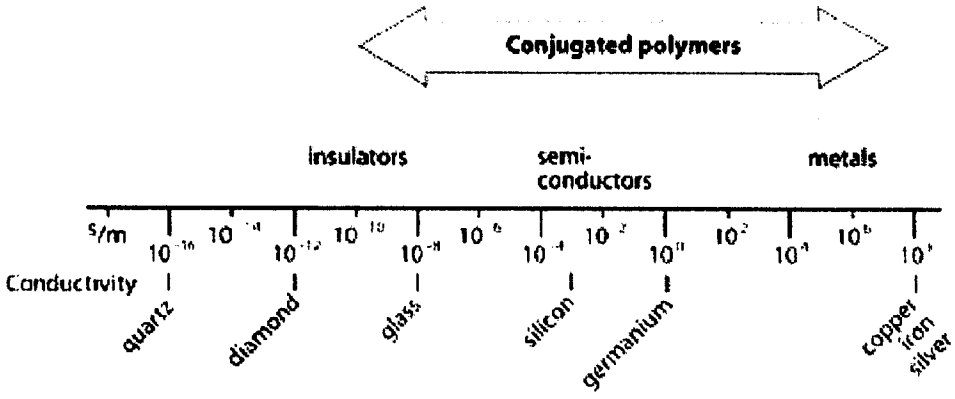


Figure 1-1 Electrical conductivities of conducting polymers [3]

The organic conductors, both the polymers and the small molecular conductors, have in common the conjugated chemical structure, i.e., alternating single and double bonds. Figure 1-2 shows the structures of the several conducting or semiconductive polymers and organics. In this conjugated structure, the carbon atoms are bonded to three other atoms, which leaves one delocalized free electron. And π orbitals of neighboring atoms overlap to form π bonds along the molecular chain, which is responsible for an important part of the intramolecular charge transport.

Many Japanese companies, such as Nippon Electric, have found polypyrrole's reversible nature of electrochemical doping suitable to be used as capacitors. Neotronics and Aromascan use polypyrrole (PPy) as chemical sensors. Researchers at Linkoping

University in Sweden are exploring the use of polypyrrole as actuators, or synthetic muscle [4].

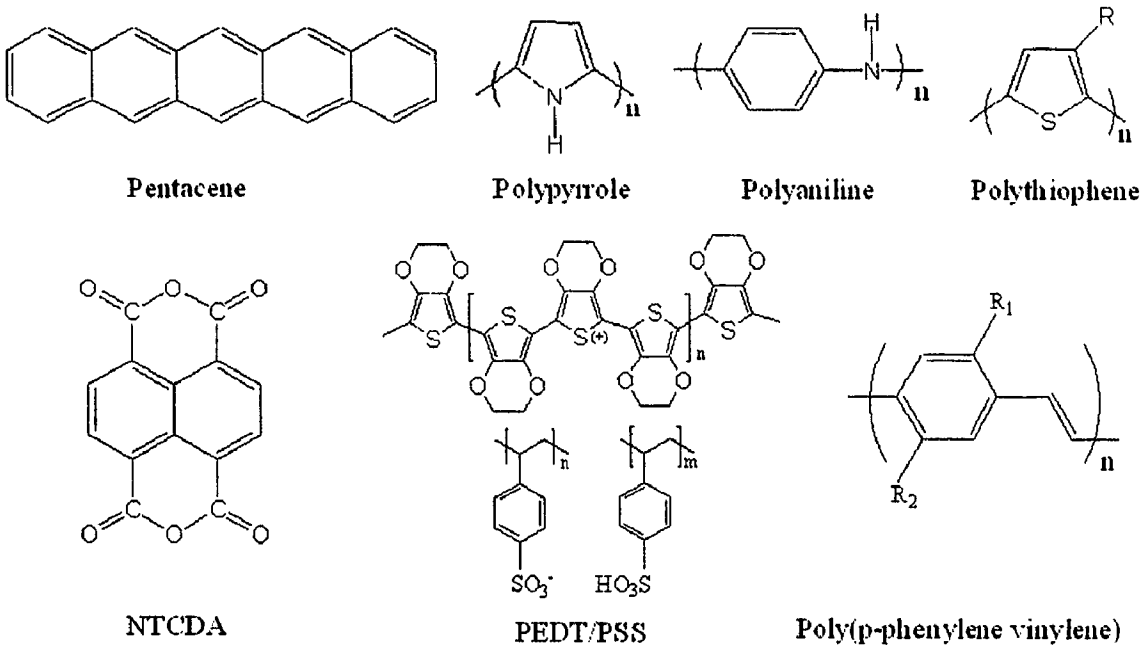


Figure 1-2 Chemical structures of conducting polymers and organics

Polythiophene has been used in light emitting diodes (LED) by several institutions such as: Bell Labs, Uniax and Philips Laboratories [4]. Polyaniline (PANI) is used in many applications similar as polypyrrole. It can also be used as a transparent electrode in LED's with a Poly(paraphenylene vinylene) (PPV) emissive layer.

PPV shown in Figure 1-2 is a basic structure of a good conductive polymer, mostly used in some derivative forms. PPV shows potential for applications in display technology from simple monochrome displays, to backlights in watches, toys, and liquid-crystal displays, to full-color LED displays [4].

Pentacene, a compound of Carbon and Hydrogen ($C_{22}H_{14}$) seems to be one of the most promising materials for organic field-effect transistors (OFETs). A sketch of the

molecule is shown in Figure 1-2. Pentacene molecules stand up vertical on the substrate, and the crystals they form can be rotated relative to each other by certain angles. Hole mobilites greater than 1 cm^2/Vs have been measured from thermally evaporated films of this material [5].

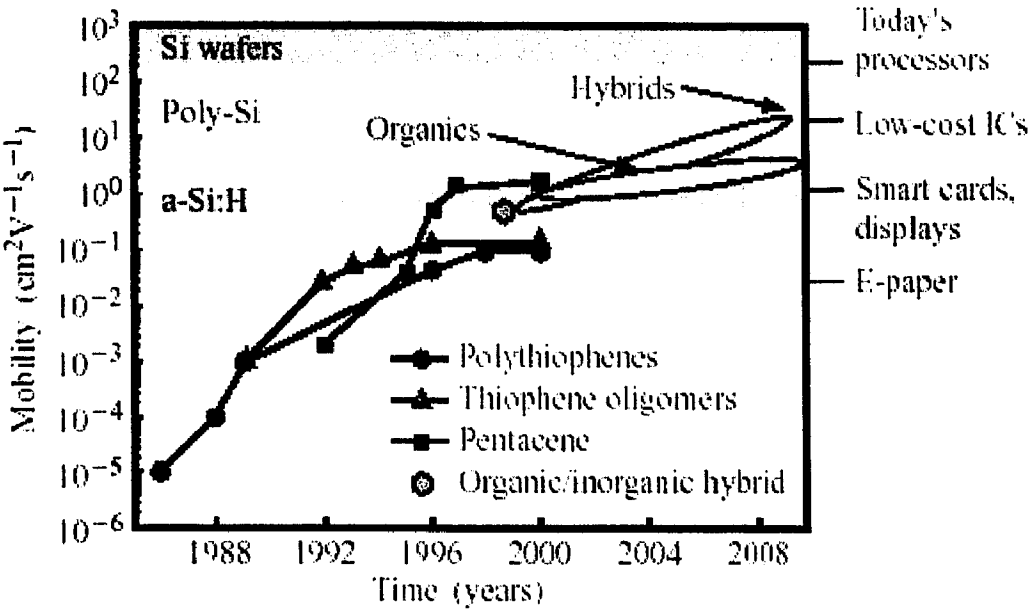


Figure 1-3 Performance of organic and hybrid semiconductors [6]

Research efforts on conducting and semiconducting polymers in academia and in industrial research laboratories have led to a dramatic improvement in performance as well as the stability and the ability to process these active materials due to innovative chemistry and processing. The mobilities of conducting polymers have been improved by five orders of magnitude over the past 20 years, as shown in Figure 1-3 [6].

Not only conducting polymers are extremely new materials, but also organic microelectronics is extremely new research field compared to the conventional silicon based microelectronics. As shown in Table 1-1, technological opportunities for

application of the conducting polymers in such diverse areas as polymer light-emitting diodes, photodetectors, flexible "plastic" transistors, electroluminescent polymer displays, chemical sensors, biosensors, to name but a few, continue to be actively pursued. Since the late 1980s, there has been a growing interest in polymer or organic microelectronics based on the conjugated polymers, oligomers, or other molecules as a result of the demonstration of high-performance electroluminescent devices and report of field-effect transistors (FETs) and organic light-emitting diodes (OLEDs). Although polymer microelectronic devices cannot rival traditional, mainstream inorganic microelectronic devices due to relatively low mobilities of the organic semiconductors, they can be competitive for the applications requiring structural flexibility, low temperature processing, large-area coverage on materials such as plastic and paper, batch production, and especially low-cost.

Table 1-1 Comparison of device based on polymer and silicon

	Polymer Device	Silicon Device
Cost	Low	High
Process Technology	Few, Simple, Low Temperature	Complicated, High Temperature
Flexiblity	Flexible	Inflexible
Device Area	Large	Small
Market	New & Growing	Mature & Almost Saturated

Among the various application of polymer microelectronics, one of the most promising applications is OLED-based active-matrix flat-panel displays [9]. Figure 1-4 shows an example of integrated polymer FET-LED for an active-matrix polymer LED pixel [9]. Japanese researchers, as well as the group at Kodak, have improved the

efficiency and the lifetime of the OLEDs to meet commercial requirements. Pioneer has produced the monochrome matrix displays for automotive applications [10].

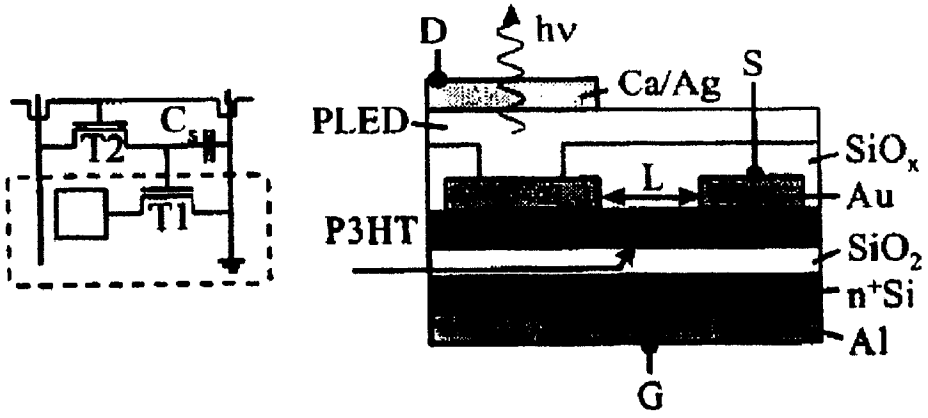


Figure 1-4 Schematic diagram of integrated polymer FET-LED [9]

Figure 1-5 Polyimide foil containing all-polymer integrated structures [11]

Another promising application of organic microelectronics is OFETs and integrated circuits. Figure 1-5 shows a photograph of a polyimide foil containing the all-polymer integrated structures fabricated by Philips in 1999 [11]. The other applications of the organic microelectronics include low-end smart cards, electronic identification tags,

photovoltaic cells, high bandwidth photodetectors [12], high density memory chips, sensors and actuators, and some pervasive computing needs. The main fabrication technologies include ink-jet printing, photochemical lithography [7], spin-coating, vacuum evaporation, soft lithography [13], and reactive ion etching (RIE).

The most serious limitations of organic microelectronic devices are the environment stability of the performance, low switching speed, high operating voltage, low-cost and batch production processing technologies. Up to now, the majority of the polymer semiconductors are p-type, transporting holes rather than electrons. And n-type semiconducting polymers are still not air-stable.

1.2 Charge Transport Mechanism

In an inorganic semiconductor like silicon, the strong coupling between the constituting atoms and the long-range order lead to the delocalization of the electronic states and the formation of allowed valence and conduction bands, separated by a forbidden energy gap. By thermal activation or photo excitation, free electrons are generated in the conduction band, leaving positively charged holes in the valence band. The transport of these free charge carriers is described by quantum mechanism.

However, the conducting or semiconducting polymers have the conjugated double bonds. The double bond consists of a σ bond and a π bond. Due to the π-orbital overlap of neighboring molecules of the conjugated structure, the electrons have gained the freedom to move along the entire chain, which provides their semiconducting and conducting properties. In metals and conventional semiconductors, charge transport occurs in delocalized states. Such a model is no longer valid in low conductivity organic semiconductors, where a simple estimate shows that the mean free path of carriers would

become lower than the mean atomic distance. The π electrons are delocalized within a molecule and the carrier transport occurs through hopping from one molecule to another.

Since the π-conjugated system extends over the whole polymer chain, the conducting polymers can be regarded as one-dimensional semiconductors. In these materials, in addition to direct electron and hole excitations across the semiconductor band gap, the one-dimensional system may support a host of exotic carrier types like solitons (topological defects without charge, with spin 1/2), polarons (electrons and holes, self-trapped by carrier-lattice interactions), soliton-polarons (charged topological defects without spin, self-trapped by carrier-lattice interactions), bipolarons (two carriers with a charge of the same sign, bound by lattice distortion), and polaron-excitons (two carriers with a charge of opposite signs, bound by lattice distortion) [14].

1.2.1 Hopping

Since 1990, there are several models being developed to rationalize the hopping transport. In most cases, the temperature dependence of the mobility follows a law of the form $\mu = \mu_0 \exp[-(T_0/T)^{1/a}]$, where a is an integer ranging from 1 to 4.

1.2.2 Small Polaron

In conjugated organic materials, the localization occurs through the formation of polarons. A polaron results from the deformation of the conjugated chain under the action of the charge. In other words, a charge is self-trapped by the deformation it induces in the chain. This mechanism of self-trapping is often described through the creation of localized states in the gap between the valence and the conduction bands.

A useful model to describe the charge transport in organic materials is that of the small polaron, developed by Holstein [15]. It is a one-dimensional, one-electron model

(that is, the electron--electron interactions are neglected). A very important parameter is the polaron binding energy E_b, which is defined as the energy gain of an infinitely slow carrier due to the polarization and deformation of the lattice. The limit of the small polaron turns up when the electronic bandwidth, 2J, is small compared to the polaron binding energy. The mobility of the small polaron is calculated by solving the time-dependent Schrödinger equation. Its high-temperature limit is given by equation

$$\mu = \sqrt{\frac{\pi}{2}} \frac{ea^2}{\hbar} \frac{J^2}{\sqrt{E_b}} (KT)^{-3/2} \exp\left(-\frac{E_b}{2KT}\right) \qquad (1\text{-}1)$$

where J is the electron transfer energy and a is the lattice constant.

1.2.3 Field-Dependent Mobility

In organic materials, a prominent feature of charge transport is that the mobility becomes field dependent at high electric field (namely, at fields in excess of $\sim 10^5$ V/cm). It occurs through a Poole-Frenkel mechanism, in which the coulombic potential near the localized levels is modified by the applied field in such a way as to increase the tunnel transfer rate between sites. The general dependence of the mobility is given by

$$\mu(F) = \mu(0) \exp\left(\frac{q}{KT} \beta \sqrt{F}\right) \qquad (1\text{-}2)$$

Here, $\mu(0)$ is the mobility at zero field, $\beta = (e/\pi\varepsilon\varepsilon_0)^{1/2}$ the Poole-Frenkel factor, and F the magnitude of the electric field.

1.2.4 Multiple Trapping and Release

Since 1991, the Thiais group has developed a charged transport model based on the multiple trapping and release (MTR) [16]. In MTR model, a narrow delocalized band is associated with a high concentration of localized levels that act as traps. During their transition through the delocalized levels, the charge carriers interact with the localized

levels through trapping and thermal release. The following assumptions are usually made: First, the carriers arriving at a trap are instantaneously trapped with a probability close to one. Second, the release of trapped carriers is controlled by a thermally activated process. The resulting drift mobility μ_D is related to the mobility μ_0 in the delocalized band by an expression of the form in

$$\mu_D = \mu_0 \alpha \exp(-\frac{E_t}{KT}) \qquad (1\text{-}3)$$

In case of a single trapping level, E_t corresponds to the distance between the trap level and the delocalized band's edge, and α is the ratio of the effective density of states at the delocalized band edge to the concentration of traps (N_t). In case of energy distributed traps, effective values of N_t and α have to be calculated.

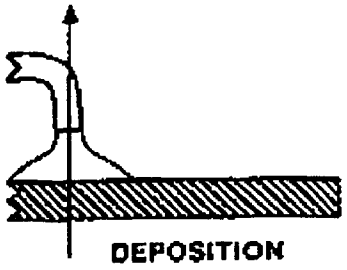
1.3 Review of Microfabrication Technologies

Polymers or organics can be deposited onto a substrate using various techniques such as spin-coating, thermal evaporation, photochemical lithography, ink-jet printing deposition, screen-printing, micromolding in Capillaries (MIMIC), and micro-contact printing (μCP). Conducting polymers can thus be reliably deposited onto microlithographically defined metallization areas on silicon wafers or devices [17].

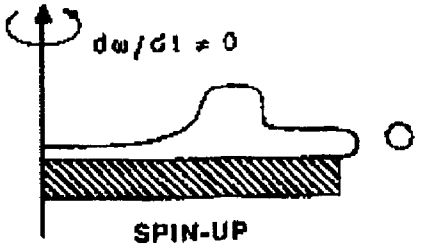
1.3.1 Spin-coating

Spin coating is generally regarded as the best way to deposit a uniform coating for many applications such as photoresist coating and dielectric/insulating layer coating. It gives optimal coverage with minimum material usage. This deposition technique is extremely desirable because the process is simple, safe, and inexpensive. In practice, spin coating involves four stages as shown in Figure 1-6 [18]. In the first stage, gravitational

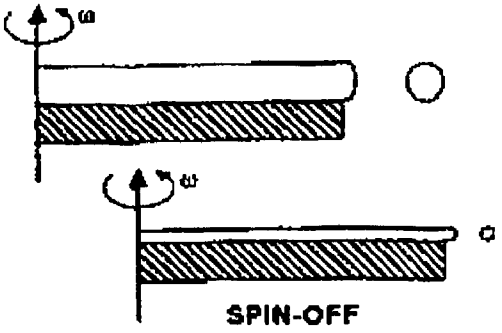
forces dominate. The surface is first wetted with excess polymer solution. In the second stage, rotational forces dominate. Film uniformity is often not present at this stage. In the third stage, viscous forces dominate. The film continues to get thinner but at a slower rate, and excess liquid continues to be expelled. In the final stage, evaporative forces dominate. Eventually, the film's thickness begins to stabilize as the evaporation of the solvent causes the viscosity of the liquid to rise sharply and overcome the centrifugal forces. What remains is an extremely thin and uniform film that is ready to be further processed. Polymer FETs fabricated with poly(benzobisimidazobenzophenanthroline) (BBL) as the n-type semiconducting material were observed to have field-effect mobilities of up to 5×10^{-4} cm^2/Vs [19].



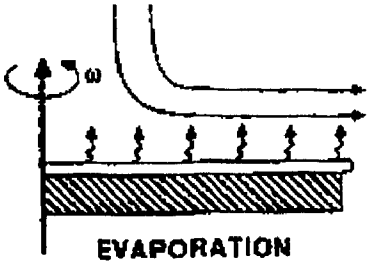
(a) First stage of spin-coating.



(b) Second stage of spin-coating.



(c) Third stage of spin-coating.



(d) Fourth stage of spin-coating.

Figure 1-6 Four stages of spin-coating process [18]

One method of depositing a polymer by spin coating is the self-induced structure formation. Firstly, two immiscible polymers are dissolved in a common solvent. The solution of the two polymers is applied to the substrate by spin coating. As the solvent evaporates, the two immiscible polymers separate. The pattern of the two polymers depends on the topography of the substrate. Then one of the polymers is removed by a selective solvent. The polymer left on the substrate will be the semiconductor or luminescent polymer in the chosen pattern.

1.3.2 Vacuum Thermal Evaporation

The vacuum thermal evaporation deposition technique consists in heating until evaporation of the material to be deposited. A scheme of the deposition equipment is shown in the Figure 1-7. The material vapor finally condenses in the form of a thin film on the substrate surface and on the vacuum chamber walls. Usually, low pressures are used, about 10^{-6} or 10^{-5} Torr, to avoid reaction between the vapor and atmosphere.

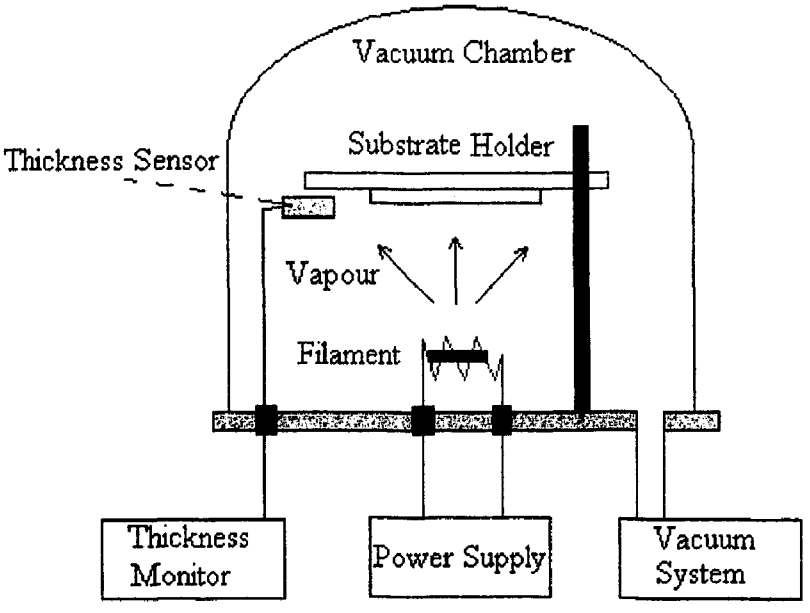


Figure 1-7 A schematic setup of the evaporator

Organic semiconducting materials can be deposited by thermal vacuum evaporation, such as 1,4,5,8-naphthalene-tetracarboxylic-dianhydride (NTCDA), and Pentacene [20][21][22][23]. By using $F_{16}CuPc$ by vacuum evaporated as n-type semiconductor, FET was reported to have a filed-effect mobility of 0.03 cm^2/Vs [24].

1.3.3 Photochemical Lithography

In 1998, Philips has developed and demonstrated all-polymer FETs by photochemical lithography for possible low-cost applications [7]. By using this technique shown in Figure 1-8, researchers in Philips Company have developed the first all polymer integrated circuits (ICs) consisting of 326 transistors with 2-μm gate length and more than 300 vertical contacts in 1998 [7].

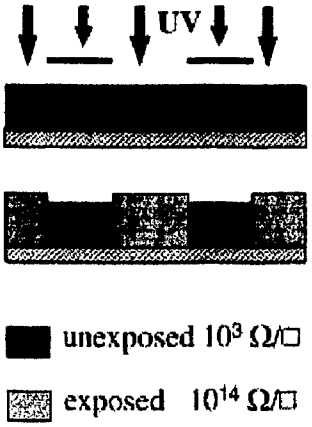


Figure 1-8 Process of photochemical lithography [7]

To use photochemical lithography, the camphorsulfonic acid doped polyaniline is dissolved in m-cresol, and a photoinitiator, 1-hydroxycyclohexylphenylketon, is added. The solution is then spin coated onto a polyimide foil substrate. In a nitrogen atmosphere, the film is exposed with deep ultra-violet (UV) light through a photomask, whereupon the conducting PANI is reduced to non-conducting leucoemeraldine. The conducting tracks

are thus embedded in an otherwise insulating matrix. The nonexposed photoinitiator in the PANI films is removed through sublimation when heated.

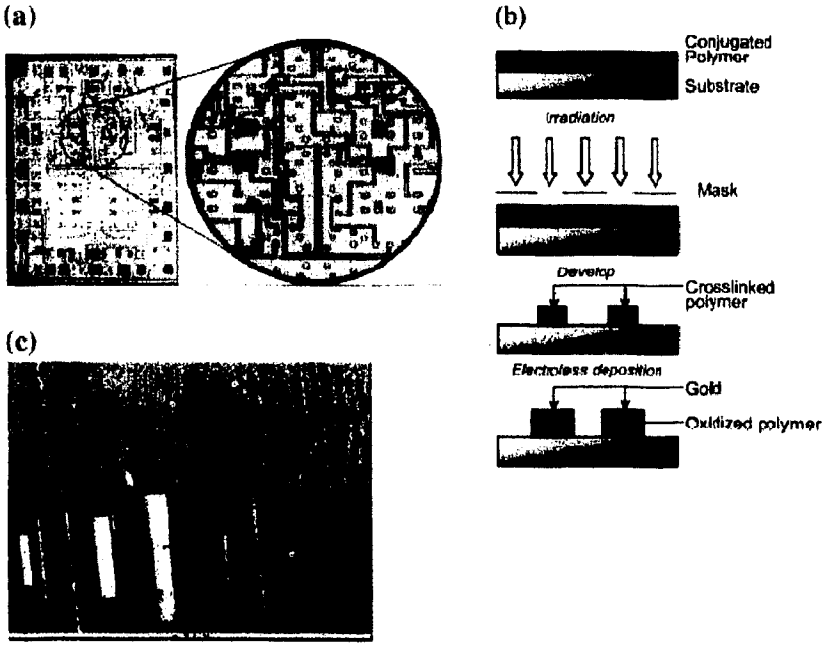


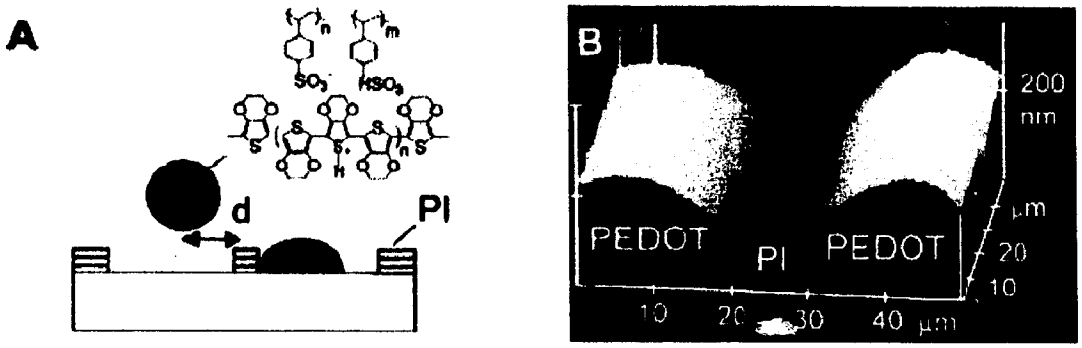
Figure 1-9 Process and optical micrograph of photo-patterned P3HT a)[25], b), c)[26]

Another well-studied class of conjugated polymer, the polythiophenes, has also been extensively studied for their photopatterning. Films of poly(3-alkylthiophenes) (P3ATs) will undergo crosslinking, becoming insoluble when irradiated with UV-vis light [25]. Figure 1-9 shows an optical micrograph of patterned poly(3-hexylthiophene) (P3HT) obtained by laser, direct-write microlithography. Conducting patterns of polythiophene have been used as a template in the electroless deposition of gold in order to fabricate micrometer-sized P3HT/Au bilayer channels [26]. Direct patterning of P3ATs can also be achieved by exposure to an electron beam [27].

1.3.4 Ink-jet Printing Deposition

Ink-jet deposition is a method in which the polymer solution takes the place of the toner in a printer. In this method the polymer pattern can be directly printed onto the

substrate. With this technique, the polymer solution can be applied to the substrate in the size of a pixel, giving very high-resolution patterns and the ability to separate pixels of red, green, and blue emitting polymers onto the substrate. Ink-jet printing has been applied to polyvinylcarbonazole (PVK)/dye composites using a commercial inkjet printer with 65 μm nozzles [28]. Ink-jet printing has also been used to deposit the conducting polymer to create dual-color light-emitting pixels [29].



(a) Schematic diagram. (b) AFM image.

Figure 1-10 Conducting polymer deposited by ink-jet printing [30]

By selectively patterning the surface regions to be hydrophobic and hydrophilic, the ink-jet printing has been used to create the OFETs and prototype integrated circuits [30]. Droplets of the water-based conducting polymer solution, poly(3,4-ethylenedioxythio-phene)/(polystyrene sulfonate) (PEDT/PSS) are deposited by ink-jet printing onto the hydrophilic regions as shown in Figure 1-10.

1.3.5 Screen-printing and Micromolding in Capillaries

Screen-printing was recently used to fabricate functional all-polymer transistors [31][32]. A schematic of the procedure for fabrication of FETs is shown in Figure 1-11. The device shown in the left of Figure 1-11 [31] was prepared from a 1.5 μm thick insulating polyester film onto which a gate was placed by screen printing a conductive

graphite-based polymer ink. For the OFETs shown to the right of Figure 1-11 [32], the solution-processable semiconducting P3AT was also deposited by screen-printing.

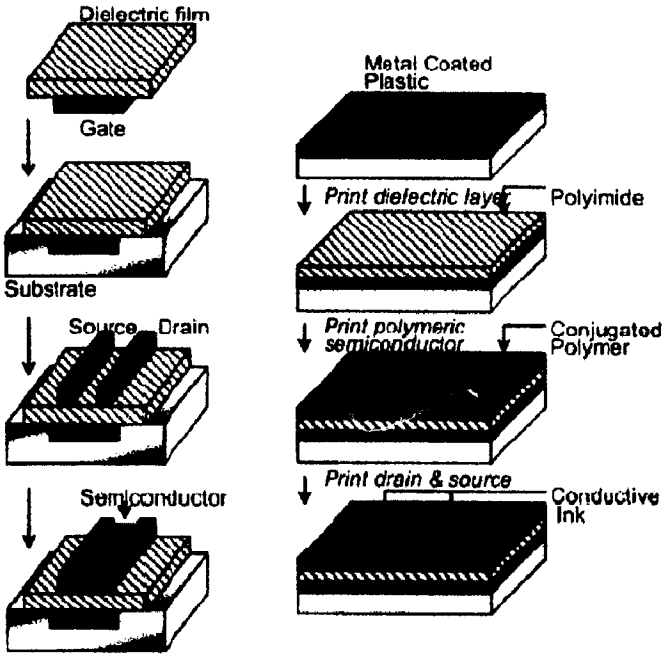


Figure 1-11 Two constructing strategies for all-polymer FETs (Left [31], right [32])

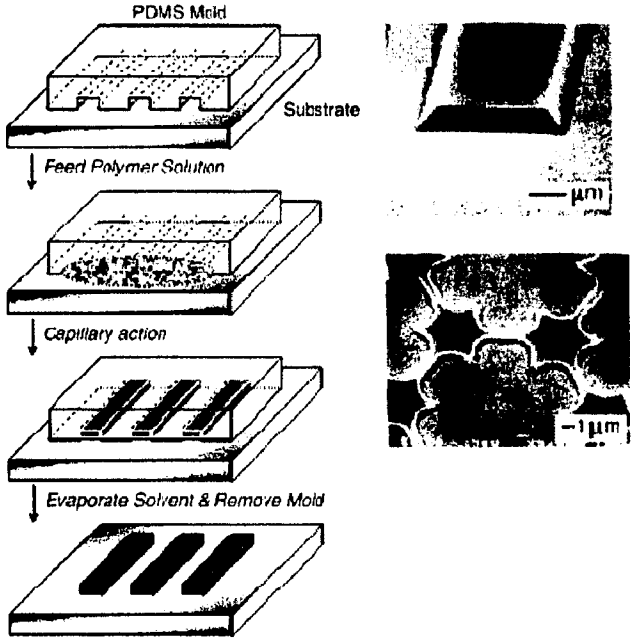


Figure 1-12 Schematic MIMIC (Left) and PANI patterns by MIMIC (Right) [33]

An alternative technique, known as MIMIC, has the ability to generate microstructures with the feature size between one and several hundred microns on a wide variety of materials. MIMIC technology derives from the class of printing methodology coined "soft lithography." The MIMIC process is illustrated in Figure 1-12, utilizing a preformed mold to possess pattern-transfer elements. The mold can be made by casting a curable elastomer, usually poly(dimethylsiloxane) (PDMS)-based, onto a master substrate possessing a negative of the desired topography, curing, and removal of the master. And these PANI patterns subsequently used as the electrodes of P3AT FETs [33].

1.3.6 Micro-contact Printing

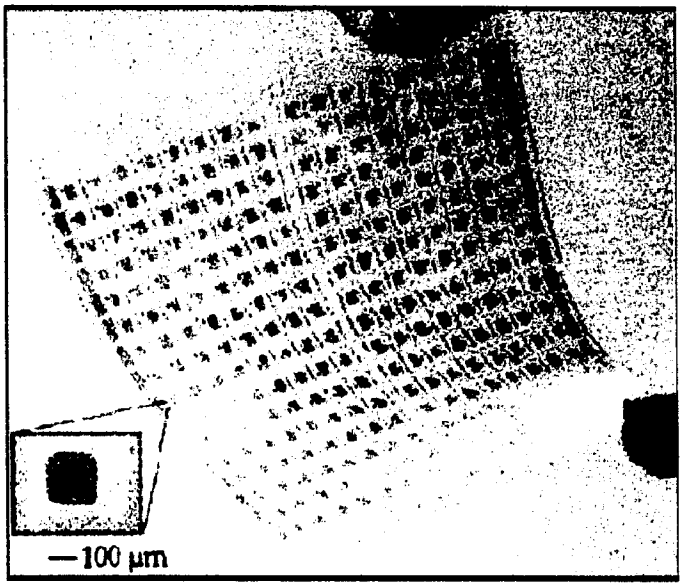


Figure 1-13 A flexible circuit containing FETs with electrodes patterned by μCP [36]

Micro-contact printing technique is based on the selective transfer of polymer material to a substrate via a PDMS stamp to obtain desired patterns or exposed and covered regions of the substrate. This can be used for the deposition of polymer materials by area-selected electropolymerization [34] or area-selected deposition [35]. Using electrodes patterned by μCP, P3HT FETs were reported to have the mobility of 0.02

cm^2/Vs. This technique has also been used to produce large area sheets containing 256 interconnected organic transistors, illustrated in Figure 1-13 [36].

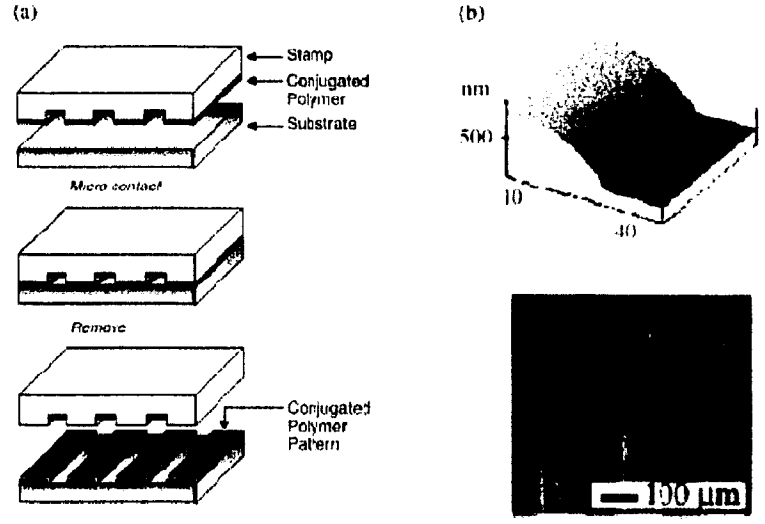


Figure 1-14 a) Schematic μCP diagram; b) AFM of patterned PEDT by μCP [37]

With the intent of patterning large areas with conducting polymer, for polymer-LEDs, the soluble PEDT/PSS conducting polymer has been deposited directly onto ITO and gold electrodes by μCP to yield conducting polymer lines 8-200 nm thick with 100 μm features, 1-2 μm edge roughness and a conductivity of ~1 S/cm [37]. An electroluminescent device using μCP technique is shown in Figure 1-14.

1.4 Research Objective

With the above overview of conducting polymer and organic microelectronic devices, it is of interest to investigate the various organic microelectronic devices fabricated with conducting and semiconducting polymers/organic by low-cost fabrication techniques, as well as the practical application of organic microelectronic devices. To benefit the advantages of organic microelectronics, on the one hand, we need to lower the

fabrication cost and simplify the fabrication processes. On the other hand, the quality and performance of the fabricated organic devices need to be improved.

In this dissertation, using traditional photolithography, reactive ion etching, nano-assembly, and ink-jet printing techniques, low-cost fabrication processes were developed to fabricate the several kinds of organic microelectronic devices, including the polymer-based Schottky diode, organic diodes based on n-type organic semiconductor and p-type semiconducting polymers, and OFETs. By using these fabrication techniques combined with the ink-jet printing technology, a simple organic integrated circuit was fabricated to demonstrate the practical application of organic devices.

1.5 Organization of this Dissertation

Chapter one, as an introduction, describes the brief overview of the history and development of conducting polymer, the various applications of organic semiconductor in organic microelectronics, followed by a discussion of fundamental physics of polymer semiconductor and carrier transport mechanism, and states the goals of this dissertation in final part. Chapter two describes how to construct Schottky diode based on the conducting polymer. Chapter three describes how to construct organic diodes with the n-type organic semiconductor and p-type semiconducting polymers. Chapter four describes how to construct PEDT/PSS OFETs based on the polymer materials. Chapter five gives the investigation of pentacene OFETs and a simple integrated circuit as an application of the organic microelectronic devices. The conclusions and the research work for future studies are addressed in chapter six.

CHAPTER TWO

POLYMER-BASED SCHOTTKY DIODE

2.1 Metal/Semiconductor Contacts

Schottky diode is one kind of fundamental device. Moreover, the study of the Schottky contact characteristics is vital for the polymer-based device because the electrical characteristics of the metal-semiconductor contact determine the device's performance. Since 1990, some attempts to fabricate metal/polymer Schottky diodes and interpret their electrical characteristics have been made [38][39][40][41][42]. However, the fabrication methods described in previous publications still appear to be complicated and the electrical characteristics of metal/polymer Schottky diodes need to be improved. The I-V curves deviated from ideality cannot be fitted by exponential equation.

When the metal contacts with the semiconductor, there will be either the ohmic contact or the Schottky contact, which depends on their material properties and the characteristics of the interface. The term "ohmic" refers in principle to a contact that is non-injecting and has a linear I-V characteristic in both directions. When metals having a lower work function than that of the semiconductor contact with the semiconductive polymer, Schottky barrier may be formed at the interface. Figure 2-1 shows the schematic energy diagram of the metal/polymer contact at zero bias. At the interface, we can find the energy level alignment and the band bending of the highest occupied

molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). Metal/semiconductor contact results in the formation of a depletion layer with a depletion width X_{dep} as shown in Figure 2-1.

In 1938, Schottky and Mott independently suggested a model for the rectification mechanism on metal-semiconductor contacts. They pointed out that the observed direction of rectification could be explained by supposing that electrons passed over a potential barrier.

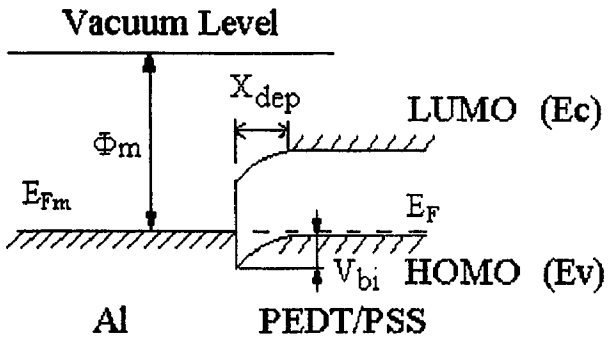


Figure 2-1 Schematic band diagram of metal/polymer contact under zero bias

The basic theory of the Schottky contact is outlined in this section. A more comprehensive description can be found in the review by Rhoderick [43][44]. The Schottky-Mott theory is expressed as:

$$\phi_{bo} = \phi_m - \chi_s \qquad (2\text{-}1)$$

where,

ϕ_{bo} = contact barrier height, at zero applied bias

ϕ_m = work function of the metal

χ_s = electron affinity of the semiconductor and is further expressed as follows:

$$\chi_S = \phi_S - (E_C - E_F) \qquad (2\text{-}2)$$

where,

ϕ_s = work function of the semiconductor

E_C = conduction band energy, in eV

E_F = Fermi energy level, in eV

ϕ_{bo} is the barrier encountered by electrons in the metal whereas the built-in potential, V_{bi}, encountered by electrons in the semiconductor, is given by:

$$V_{bi} = \phi_m - \phi_s = \phi_{bo} - (E_C - E_F) \qquad (2\text{-}3)$$

2.2 Current-Voltage Measurements

2.2.1 Theory

Current-voltage (I-V) measurements of polymer-based Schottky diode refer to d.c. characterization for the purposes of performance analysis and parameter extraction.

The current transport through the device by emission over the barrier can be considered as a two-step process: firstly, the electrons have to be transported through the depletion region, which is determined by the usual mechanisms of diffusion and drift; secondly, they must undergo emission over the barrier into the metal. The current voltage relationship of Schottky diode is expressed as:

$$I = AA^*T^2\exp(-q\phi_{bo}/kT)(\exp\{-qV_{eff}/nkT\} - 1) \qquad (2\text{-}4)$$

where,

A = cross-sectional area of the metal/semiconductor interface

A* = modified Richardson constant for metal/semiconductor interface

T = absolute temperature in kelvins

q = electronic charge

k = Boltzmann constant

V_{eff} = effective bias across the interface

n = ideality factor

This mode of current transport is commonly referred to as the "thermionic emission" current [45]. In addition to the thermionic emission, there are a number of other effects and current transport mechanisms that also contribute to the electrical properties of the metal/semiconductor's interface.

2.2.2 Important Schottky Diode Parameters

There are three important parameters that affect much of the performance of Schottky diode: barrier height, ideality factor, and series resistance. There are some publications dealing with the influence and the extraction of these parameters [46][47].

Barrier height (ϕ_{bo}) is defined as the potential difference between the Fermi energy of the metal and the band edge where the majority carriers reside. It is also the potential barrier to thermionic emission that naturally exists between an intimate metal and semiconductor contact at zero applied bias.

The ideality factor, n, gives a measure of the quality of the junction that is highly process dependent. For an ideal Schottky junction, n = 1. However, larger values are often obtained due to the presence of non-ideal effects. The ideality factor can also be obtained from the slope of the curve on a semi-logarithmic scale in units of V/decade.

The series resistance (Rs) of the diode affects the forward biased *I-V* characteristics of real diodes. For high forward bias voltages, the current of the diode no longer increases exponentially with the voltage. Instead, it increases linearly due to the series resistance of the diode. This series resistance may be due to the contact resistance between the metal and the semiconductor, the resistivity of the semiconductor, or the series resistance of the connecting wires. The series resistance could be determined from I-V plot where at high current, the plot becomes flat and is dominated entirely by the Rs. Thus, from the plot of I-V, Rs could be extracted from the point where the curve saturates to a steady minimum value.

2.3 Capacitance-Voltage Measurements

Capacitance versus voltage, referred to as C-V, measurements can be used to study the basic properties of semiconductor rectifying junctions. In addition to obtaining simple capacitance values at a given bias, the data can be manipulated to yield a number of other parameters such as the built-in potential, V_{bi}, the doping concentration [48] and the barrier height [49].

2.3.1 Theory

From Poisson's analysis, the depletion width of an abrupt p-n junction is given by:

$$X_{dep} = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q} \cdot \frac{N_A + N_D}{N_A \cdot N_D} \cdot (V_{bi} - V_A)} \qquad (2\text{-}5)$$

where,

X_{dep} = depletion width of an abrupt p-n junction

ε_0 = dielectric constant of free space

ε_r = dielectric constant of the semiconductor material

q = electronic charge

N_A = acceptor doping density in the p-region

N_D = donor doping density in the n-region

V_{bi} = built-in potential

V_A = applied bias

To take an n-type Schottky junction as the example, the above equation can be simplified to be:

$$X_{dep} = \sqrt{\frac{2\varepsilon_O \varepsilon_r}{qN_D} \cdot (V_{bi} - V_A)} \qquad (2\text{-}6)$$

The junction capacitance of the devices is approximated by:

$$C = \frac{\varepsilon_O \varepsilon_r}{X_{dep}} A \qquad (2\text{-}7)$$

From equation 2-6 and equation 2-7, the following relationship between C and V_A can be derived:

$$\frac{1}{C^2} = \frac{2}{qN_D \varepsilon_O \varepsilon_r A^2} (V_{bi} - V_A) \qquad (2\text{-}8)$$

When the measured C-V data were plot as a graph of $1/C^2$ versus V_A, the built-in potential, V_{bi}, can be yielded from the x-axis intercept.

By differentiation of equation 2-8 with respect to V_A, the doping concentration for the semiconductor, N_D, can be determined using the following equation:

$$N_D = [2/(q\varepsilon_o\varepsilon_r A^2)]\frac{dV_A}{d\left(\frac{1}{C^2}\right)} \qquad (2\text{-}9)$$

2.3.2 Limitations

C-V measurements suffer from a number of fundamental limitations [50]. These include the total depth that can be profiled before the onset of avalanche breakdown and the validity of the depletion approximation. Furthermore, the two requirements for the depletion approximation, that the depletion region be free from mobile charge and have an abrupt boundary, are hard to satisfy in practice.

As seen from the above equations, the accurate junction area is crucial to C-V measurements. In addition, they are also vulnerable to erroneous interpretation, particularly due to series resistance and parasitic capacitance as well as those arising from the device geometry [51].

2.4 Experimental Set-up

The experimental set-up for current-voltage measurements and capacitance-voltage measurements essentially consists of a probe station with a microscope, a Keithley Test System with ICS (Interactive characterization software) and a personal computer (PC). The probe station is connected to the Keithley Test System via a set of cables enabling the measurement of a number of d.c. parameters. The Keithley Test System is in turn connected to the PC by an IEEE interface allowing data transfer. A schematic diagram of the set-up is shown in Figure 2-2.

The probe station connected with Keithley measurement system was made by Micromanupulator Corporation. Keithley measurement system includes the 236, 237, and

238, KI595, and K590 Source-Measure Units (SMU). It can measure the characteristics of resistor, diode, capacitor, bipolar transistor, and MOSFET. The 236, 237, and 238 units are fully programmable instruments, capable of sourcing and measuring voltage or current simultaneously. The KI595 and K590 units are capable of capacitance-voltage measurement. The frequency range for the test signal is 100 kHz to 1 MHz.

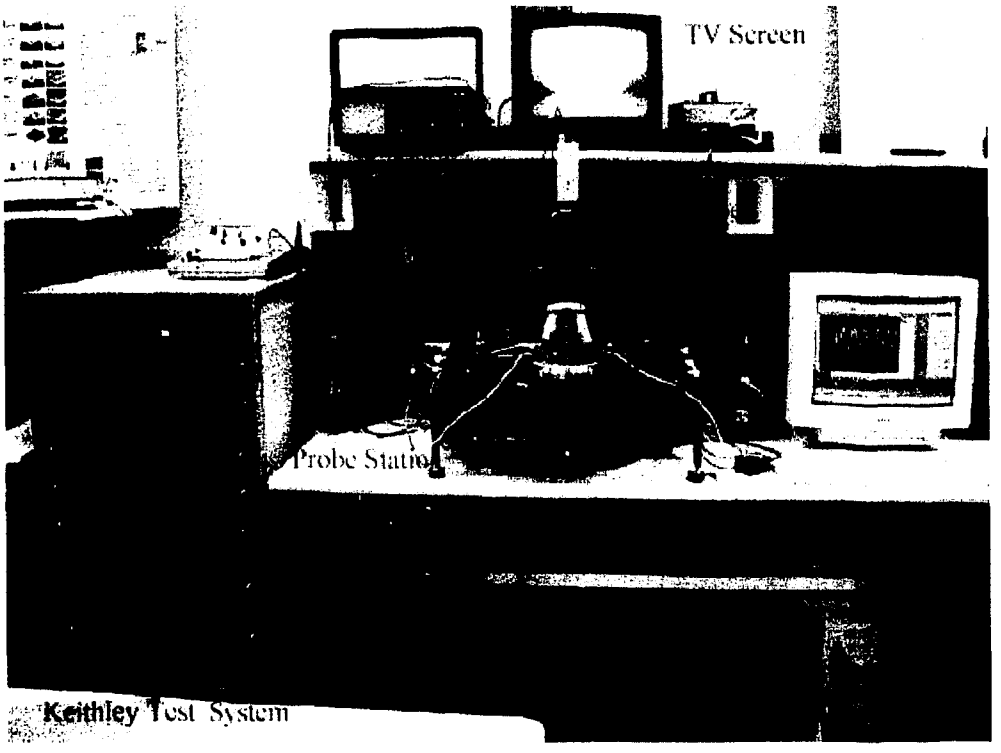


Figure 2-2 Schematic diagram of set-up for I-V and C-V measurements

ICS is a powerful instrumentation control and data analysis software package. ICS is designed to control semiconductor test equipment used for device characterization and other microelectronics testing. Selecting instrument drivers, and creating test setups are all completed while in the measurement mode. Files exported as ASCII data are readable text files only, which can be analyzed by Microsoft Excel or similar software. Appropriate programming of the SMUs enables the user to perform a wide range of

operations on the device. The maximum current that can be sourced from SMUs is 100 mA while the minimum measurable current is on the order of 10^{-15}A, thus lending itself to good use for most d.c. parameter extractions.

2.5 Experimental of Al/(PEDT/PSS) Schottky Diodes

2.5.1 Resistivity Measurement of PEDT/PSS Thin-Film

In this experiment, the arrangement of two-parallel electrodes methods shown in Figure 2-3 was used to measure the resistivity of PEDT/PSS thin-film. Fluke 87 TrueRMS Multimeter and Keithley 235 Source Measurement Unit (SMU) were used to measure the resistance between two metal electrodes.

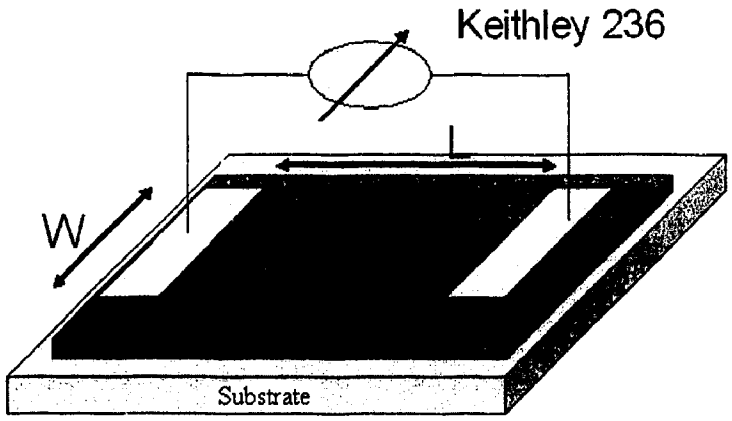


Figure 2-3 Parallel electrodes set-up for PEDT/PSS resistivity measurement

After the silicon substrate with SiO_2 is cleaned and baked at 150 °C for 15 minutes, PEDT/PSS solution was spin-coated. PEDT/PSS thin-film was formed after the sample was baked on a temperature-controlled hot plate at 120°C for 5minutes. Then, a layer of Au electrode with the thickness of 100 nm and 8nm thick Cr as an adhesion layer were sputtered on PEDT/PSS film to form two-parallel electrodes using a shadow mask. The thickness of the PEDT/PSS thin-film, d, is about 1.4 μm from the measurement by

Tencor step profile instrument. The dimensions of the two Au electrodes are: 37 mm long (W), 5 mm wide, and 25 mm apart (L).

Approximate resistance, R, measured with Fluke 87 TrueRMS Multimeter was of 6.22 Kohm. The resistivity ρ can be calculated to be 1.289 Ω·cm from the resistance (R) according to the equation 2-10:

$$\rho = \frac{RWd}{L} \qquad (2\text{-}10)$$

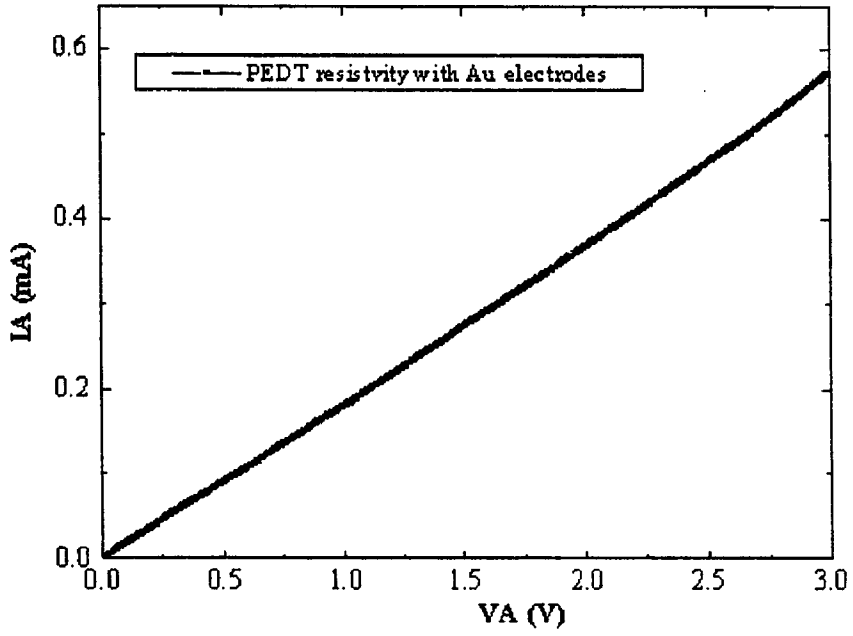


Figure 2-4 I-V Curve of PEDT thin-film with Au electrodes

From the experimental data shown in Figure 2-4 measured by Keithley 236 SMU, the resistance between two Au electrodes could be found to be 5.321 Kohm. Thus, the resistivity of PEDT/PSS thin-film can be calculated to be 1.103 Ω·cm from the equation 2-10. The surface resistivity of PEDT/PSS thin film is found to be:

$Rs=R\times W/L=7.88\times10^{3}$ Ω/Square

In a similar way, the PEDT/PSS thin-film was prepared for resistivity measurement except the thermal evaporated Al as the two-parallel electrodes instead of the sputtered Au. Al was thermally evaporated at a rate of 2 Å/sec until a final electrode-thickness of 1200 Å is reached. The dimensions of Al electrodes are: 1.1 cm long (W), 2 mm wide, and 1.6 cm apart (L). The thickness of the PEDT/PSS thin-film, d, is about 1.02 μm from the measurement by Tencor step profile instrument.

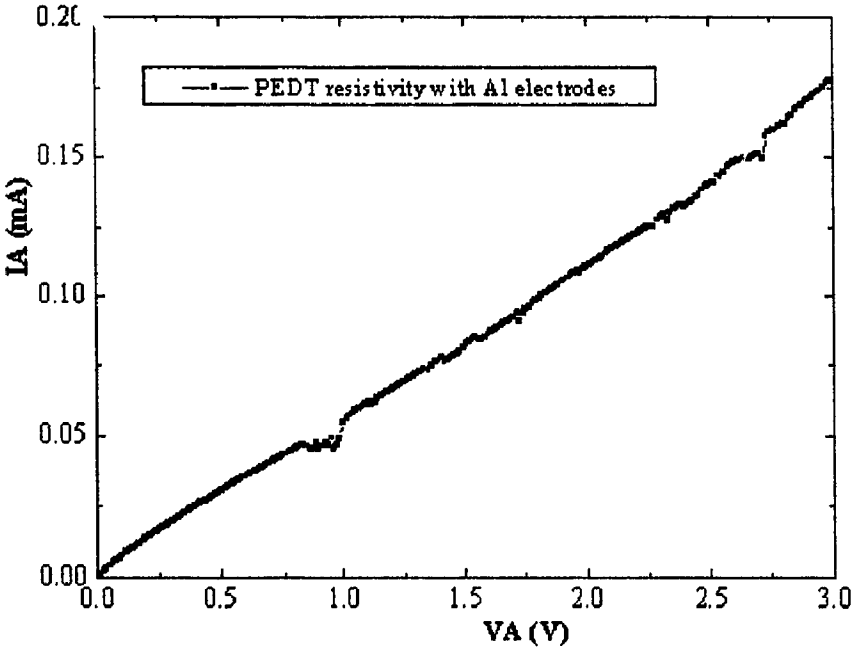


Figure 2-5 I-V Curve of PEDT thin-film with Al electrodes

Approximate resistance, R, measured with Fluke 87 TrueRMS Multimeter was of 29 Kohm. The resistivity ρ can be calculated to be 2.03 Ω·cm from the resistance according to the equation 2-10. By measuring with Keithley 236 SMU, the resistance between two Al electrodes could be found to be 18 Kohm from the Figure 2-5. Thus, the resistivity of PEDT/PSS thin-film can be calculated to be 1.26 Ω·cm from equation 2-10. The surface resistivity of PEDT/PSS thin film is found to be:

$Rs=R\times W/L=1.24\times10^4$ Ω/Square

Through the above measurements, we obtained the value of the approximate volume resistivity of 1.1 Ω·cm and the surface resistivity of 1×10^4 Ω/Square for the PEDT/PSS film. These values are close to the values provided by Baytron (Vender) for unmodified Baytron P coatings, 1 Ω·cm and around 10^4 to 10^6 Ω/Square, respectively.

2.5.2 Fabrication of Al/(PEDT/PSS) Schottky Diodes

To fabricate the polymer Schottky diode, heavily doped silicon wafer was used as an electrode (resistivity of about 0.01 Ω·cm). PEDT/PSS (Baytron P), functioning as the semiconductive layer, was then deposited on the silicon substrate by spin-coating with a thickness of 1 μm. Upon finishing the spin-coating, the PEDT/PSS film was cured for 5 minutes at 120°C and then slowly cooled down to room temperature in order to minimize the thermal stress. Then a 150 nm thick aluminum film was thermally evaporated on the PEDT/PSS film in vacuum. At last, the polymer Schottky diodes were formed by the RIE technology with Al as the mask that can avoid the chemical attack from the solution. Figure 2-6 shows the schematic diagram of resulted polymer Schottky diode structure. The fabrication procedure of Al/(PEDT/PSS) diode can be described in detail in Fig. 2-7.

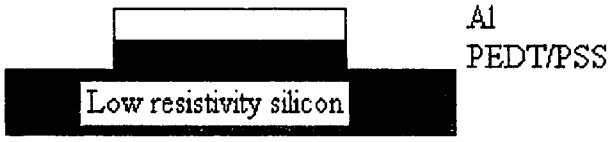
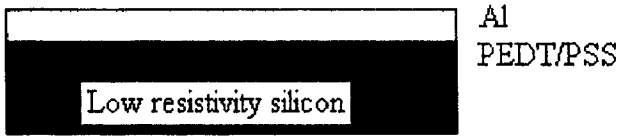


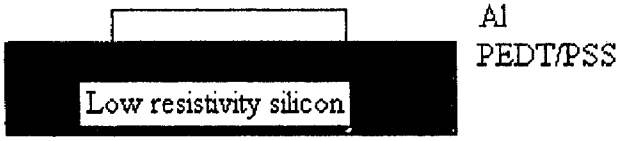
Figure 2-6 Schematic diagram of polymer Schottky diode structure

(a) Prepare for low resistivity silicon wafer.

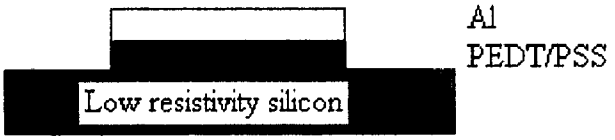
(b) Spin-coat a layer of PEDT/PSS: 1μm.



(c) Thermally evaporate a layer of Al: 200nm.



(d) Pattern Al using photolithography.



(e) Pattern PEDT/PSS by RIE etching

Figure 2-7 Schematic fabrication process of Al/(PEDT/PSS) Schottky diode

2.6 Results of Al/(PEDT/PSS) Schottky Diodes

The electrical characteristics of the Al/(PEDT/PSS) Schottky diode were measured point-by-point with one minute intervals to approach a steady-state condition

and analyzed by the thermionic emission theory of the Schottky barrier. The current as a function of applied bias V is given by equation 2-11 when the forward bias V>3kT/q:

$$I = I_S \exp(qV / nkT) \qquad (2\text{-}11)$$

where I_S, the saturation current that could be obtained from the extrapolation of the linear portion of lnI-V plot, is given by:

$$I_S = AA^*T^2 \exp(-q\phi_B / kT) \qquad (2\text{-}12)$$

where A is the contact area, A* is the effective Richardson constant ($120 A/K^2cm^2$), k is the Boltzmann's constant, T is the absolute temperature, ϕ_B is the barrier height, and q is the elementary charge.

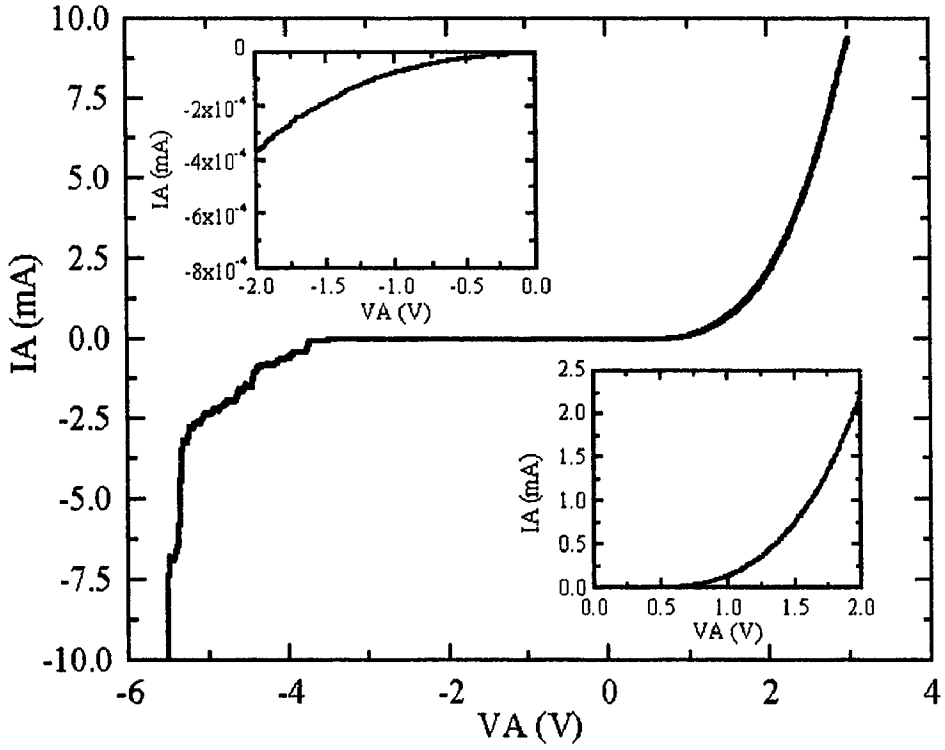


Figure 2-8 I-V characteristics of Al/(PEDT/PSS) contact

Figure 2-8 shows the I-V characteristics of the Al/PEDT contact. The breakdown voltage of the diode is shown to be about 5.5V, which is much lower than the silicon diode but almost three times higher than the breakdown voltage of the Al/PPy (doped polypyrrole) Schottky diode [38]. Due to the low conductivity of the PEDT/PSS polymer, the measured I-V curve shows an excessive series resistance, and the conventional I-V extraction method for parameters like barrier height does not work well in this case. Here, the modified Norde function method was used to determine the barrier height while overcoming the series resistance problem.

The modified Norde function [52] F(V) is defined as

$$F(V) = \frac{V}{\alpha} - \frac{1}{\beta}\ln\left[\frac{I(V)}{AA^{*}T^{2}}\right] \qquad (2\text{-}13)$$

where I(V) is from the measured I-V curve, α is an integer greater than 1, and β is a temperature-dependent value calculated with equation 2-16. For a series of value α, we can obtain a series of corresponding minimum values for F(V) from:

$$V_A = V - IR_S \qquad (2\text{-}14)$$

$$I = I_S \exp\left(\frac{V_A\beta}{n}\right) \qquad (2\text{-}15)$$

$$\beta = q/kT \qquad (2\text{-}16)$$

where V_A is the voltage applied on the barrier region. We can then derive the following equation:

$$I_\alpha = \frac{1}{R_s\beta}\alpha - \frac{n}{R_s\beta} \qquad (2\text{-}17)$$

Once we know the minimum values of F(V), the corresponding $I_\alpha \sim (\alpha/\beta)$ curve can be plotted as shown in Figure 2-9. From the slope, the value of series resistance, R_S, can be calculated to be 7.34 Ohm. By extrapolating the $I_\alpha \sim (\alpha/\beta)$ curve, we can also calculate the value of the ideality factor of the polymer-based Schottky diode, n=1.42. Based on the calculated R_S and n values, we can plot an $I \sim V_A$ curve and obtain the Schottky barrier height by using the traditional I~V method. Using this method, the Schottky barrier height is determined to be 0.97 eV. The rectification ratio is determined to be 1.3×10^4 at 1.5 V, which is attributed to the Al/PEDT interface.

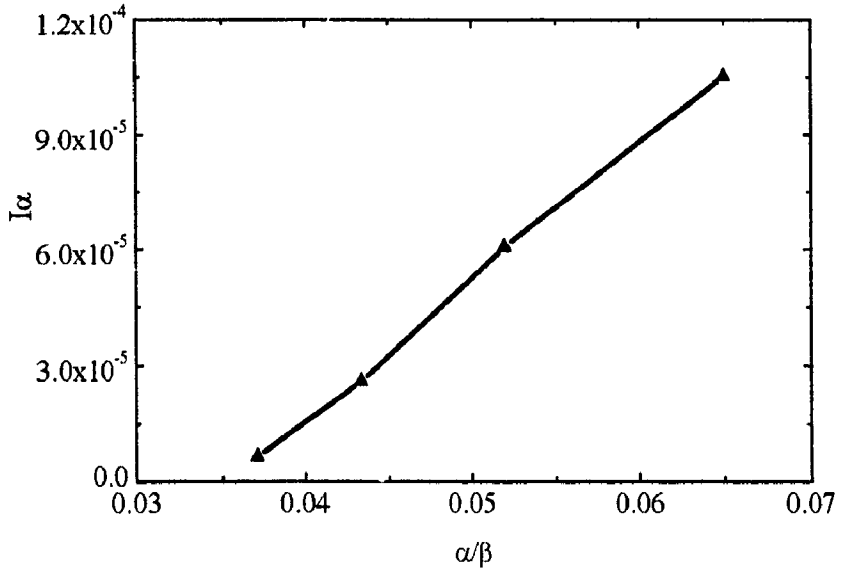


Figure 2-9 $I_\alpha \sim (\alpha/\beta)$ Curve

To further the study of the junction properties, the bias-dependent capacitance was investigated at a fixed frequency of 100 kHz. Figure 2-10 shows the capacitance-voltage characteristics of the Al/PEDT Schottky diode under small reverse bias. According to Schottky's theory, the depletion layer capacitance is given by:

$$C^{-2} = 2[V_D + V_R - (kT/q)]/q\varepsilon_0\varepsilon NA^2 \qquad (2\text{-}18)$$

where C is the capacitance, V_R is the applied reverse bias, q is the electronic charge, A is the device area, N is the hole-carrier concentration, and $\varepsilon_0\varepsilon$ is the dielectric constant of a semiconductor. We can find the carrier concentration from the slope of linear part in Figure 2-10 according to equation 2-19:

$$N = (2/q\varepsilon_o\varepsilon A^2)\frac{dV}{d\left(\frac{1}{C^2}\right)} \qquad (2\text{-}19)$$

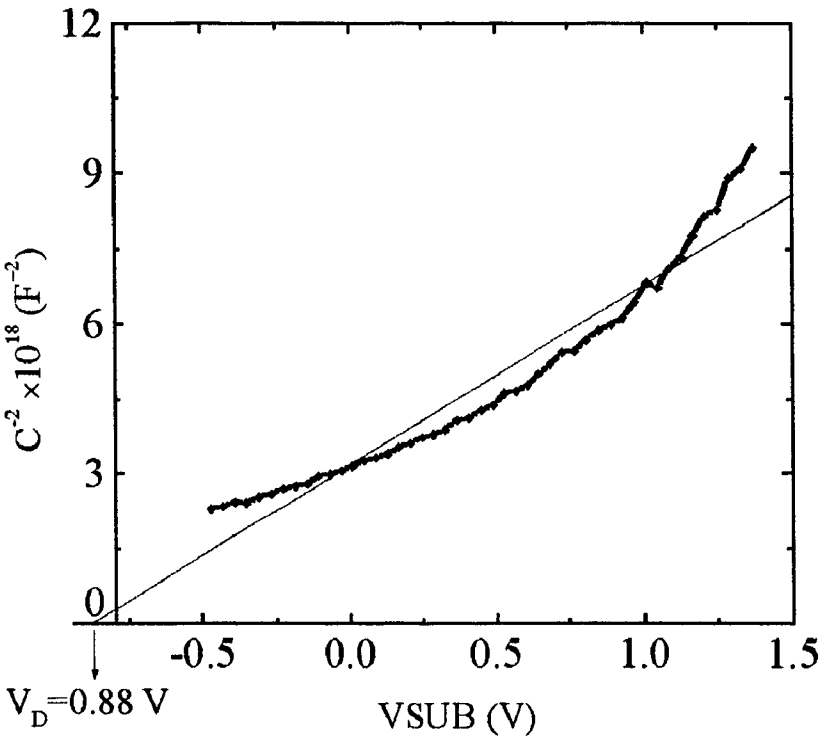


Figure 2-10 Reverse bias C^{-2}~V plot of Al/(PEDT/PSS) Schottky diode

Assuming ε=3 [53], the approximate carrier concentration is found to be about 2.09×10^{18} cm^{-3}. The nonlinearity shown in Figure 2-10, which indicates a non-uniform

dopant density profile, is attributed to the interface states introduced by the interfacial layer and the surface irregularities that cause the variation of the effective area. The voltage axis intercept of the C^{-2}-V plot gives a value of about 0.88 V for diffusion voltage, V_D. The work function of Al is 4.28 eV. From the equation $\phi_S - \phi_m = V_D$, the work function of PEDT/PSS is found to be 5.16 eV. We know the bandgap of PEDT/PSS is 1.6 eV [54], thus from the barrier height and V_D, Fermi level E_F is obtained to be 0.09 eV above valence band or HOMO.

In summary, a polymer-based PEDT Schottky diode has been fabricated by using simple spin coating and RIE technologies, and the I-V characteristics and the bias-dependent capacitance of the diodes have been studied. The electrical parameters are extracted by the modified Norde function method in which the effects of the series resistance and the ideality factor have been taken into account. Al/PEDT diode has a relatively high breakdown voltage of about 5.5 V and a rectification ratio of about 1.3×10^4. In addition, the Fermi level and the carrier concentration of the PEDT/PSS have been determined.

In this chapter, two macroscopic methods, I-V and C-V characteristics based on electrical measurements, were used to study the polymer based Schottky diode and its interfacial properties. Some future works and deeper analysis may be pointed out: better analysis techniques, such as UPS, XPS, and Kelvin probe method, should be applied to study the electronic structures of the materials and the interface structures of metal-semiconducting polymer contact so that better understanding for interfacial energy level alignment and band bending could be achieved.

CHAPTER THREE

ORGANIC DIODES

3.1 Introduction

The p-n diodes can be used as a rectifier, as an isolation structure and as a voltage-dependent capacitor. In addition, they can be used as solar cells, photodiodes, light emitting diodes, and even laser diodes.

Up to now, many efforts have been taken for the preparation and characterization of metal/organic Schottky junctions and photodiodes [38][40][55][56]. Some researchers have attempted to fabricate the organic p-n junction by electrochemical or photochemical processes [57]. However, there are few reports on the fabrication and properties of junctions based on two different types of organic semiconductors with the lithographic technique. In this chapter, the basic theory of organic/organic contact will be briefly introduced first, then the low-cost fabrication process and the electrical characteristics of two kinds of organic diodes will be presented in detail.

3.2 Organic/Organic Contact

A p-n junction consists of two semiconductor regions with opposite type as shown in Figure 3-1. We will assume, unless stated otherwise, that the doped regions are uniformly doped and that the transition between the two regions is abrupt. Figure 3-1 shows the junction biased with a voltage V_a.

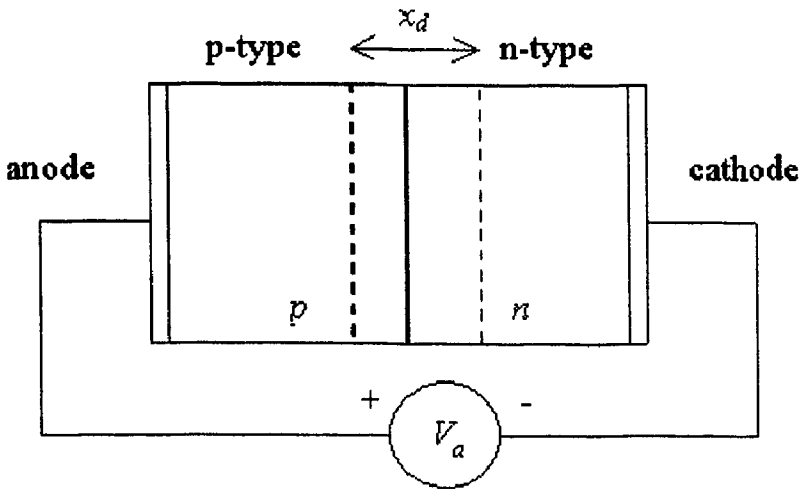


Figure 3-1 Cross-section of a p-n junction

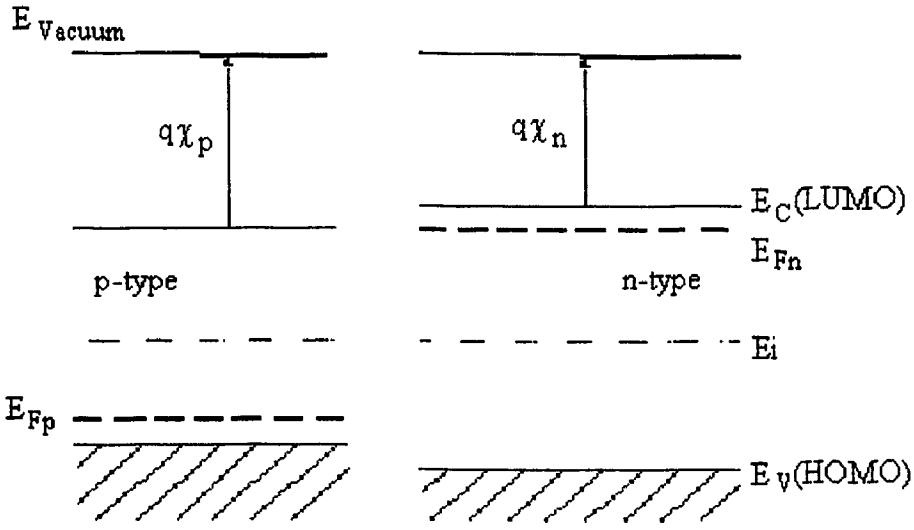


Figure 3-2 Band diagram of a p-n junction before contact

Figure 3-2 shows the schematic energy diagram of an n-type semiconductor and a p-type semiconductor before contact. When both semiconductors are brought together, they will align their energy band by bending the band to reach a thermal equilibrium as shown in Figure 3-3. At thermal equilibrium, electrons/holes close to the metallurgical junction and they diffuse across the junction into the p-type/n-type region, creating a

region around the junction called the depletion region. The diffusion of carriers continues until the drift current balances the diffusion current, thereby reaching thermal equilibrium.

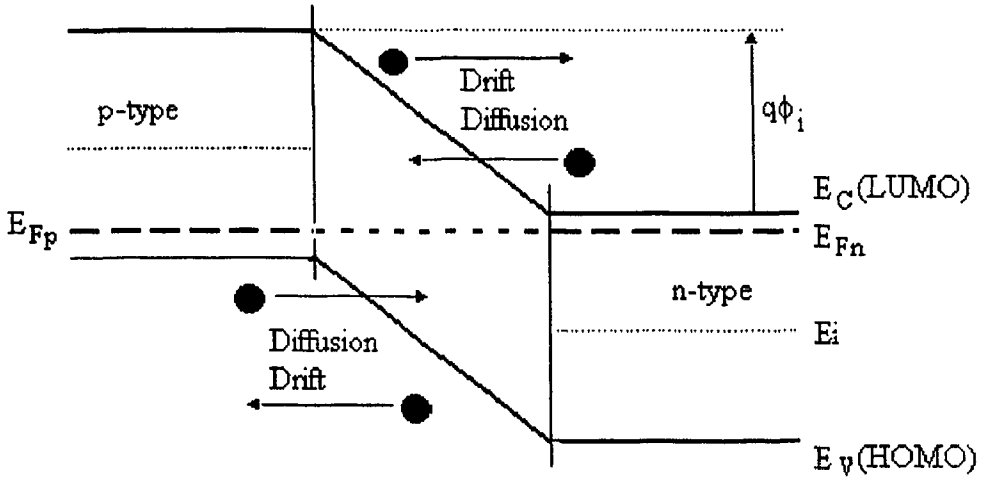


Figure 3-3 Energy band diagram of a p-n junction in thermal equilibrium

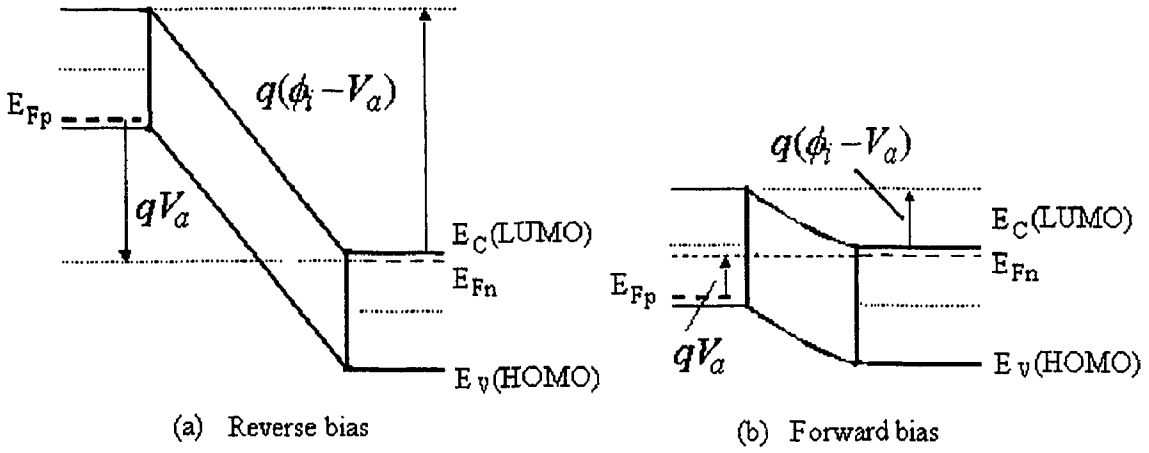


Figure 3-4 Energy band diagram of a p-n diode under forward bias and reverse bias

While no external voltage is applied between the n-type and p-type material in thermal equilibrium, there is an internal potential, ϕ_i, between the n-type and p-type

semiconductors. This potential equals the built-in potential. Both bias modes are illustrated with Figure 3-4. The applied voltage is proportional to the difference between the Fermi energy in the n-type and p-type quasi-neutral region.

3.3 Current – Voltage Measurements

The electrostatic analysis of a p-n diode is of interest since it provides knowledge about the charge density and the electric field in the depletion region.

The general analysis starts by setting up Poisson's equation with the assumption that the depletion region is fully depleted and the adjacent neutral regions contain no charge. The full-depletion approximation assumes that the depletion region around the metallurgical junction has a well-defined boundary. It also assumes that the transition between the depleted and the quasi-neutral region is abrupt.

The current in a p-n diode is due to carrier recombination or generation somewhere within the p-n diode structure. Under forward bias, the diode current is due to recombination. This recombination can occur within the quasi-neutral semiconductor, within the depletion region or at the metal-semiconductor Ohmic contacts. Under reverse bias, the current is due to generation. The total current must be constant throughout the structure since a steady state case is assumed. The total current is then given by:

$$I = AJ \cong I_S(e^{qV_a/KT} - 1) \qquad (3\text{-}1)$$

where I is the diode current, A is junction area, J is the diode current density, I_s is the saturation current, V_a is the applied voltage, K is Boltzmann's constant and T is the absolute temperature.

The maximum reverse bias voltage that can be applied to a p-n diode is limited by breakdown. Breakdown is characterized by the rapid increase of the current under reverse bias. The corresponding applied voltage is referred to as the breakdown voltage. The breakdown voltage is a key parameter of a p-n diode.

3.4 Fabrication of Organic Diodes

PEDT/PSS, NTCDA, and PPy have attracted much attention as new organic electronic materials applicable to microelectronic devices. PEDT/PSS is an optically transparent p-type semiconducting polymer [58]. PPy is an air-stable, solution processable p-type semiconducting polymer and has very good mechanical strength [59]. NTCDA is a widely used n-type organic semiconductor.

Figure 3-5 shows the schematic structure of the organic diodes with aluminum as the RIE mask. To fabricate organic diodes, an n-type heavily doped silicon wafer with a low resistivity of about 0.001 Ω·cm was used as an electrode and substrate. Due to the moisture sensitivity of NTCDA, after cleaning the silicon substrate, a layer of undoped NTCDA 600 nm thick was thermally evaporated in a vacuum chamber (about 1×10^{-7} Torr) at a low deposition rate at room temperature to improve the film crystalline quality.

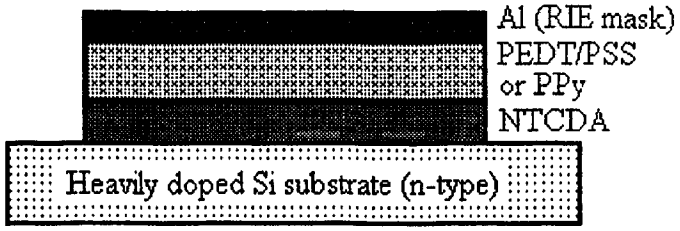
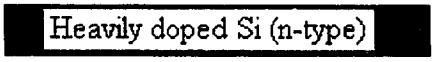
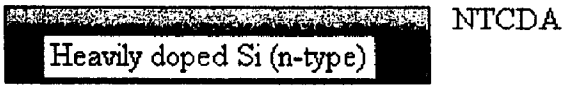


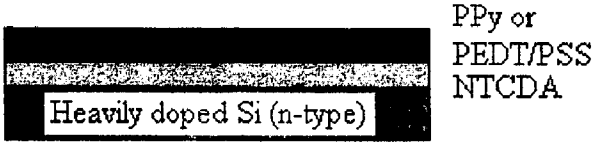
Figure 3-5 Schematic structure of organic diodes with Al as RIE pattern mask



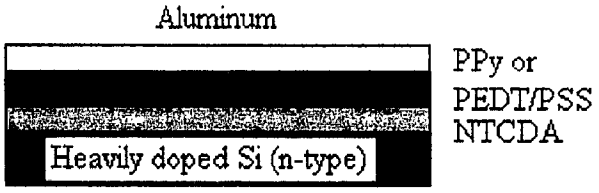
(a) Prepare the heavily doped silicon substrate (n-type).



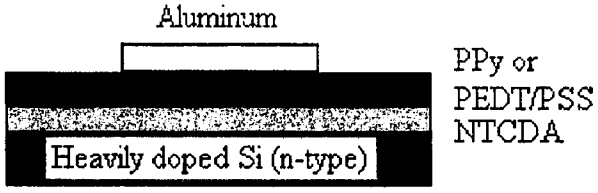
(b) Evaporate NTCDA.



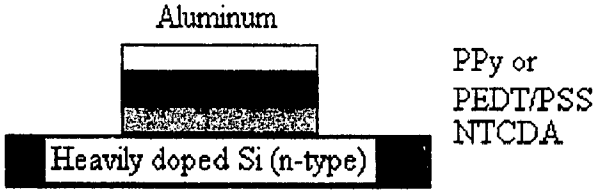
(c) Spin-coat PPy or PEDT/PSS.



(d) Thermally evaporate a layer of Al: 150nm.



(e) Pattern Al by wet etching.



(f) Pattern PPY and NTCDA layers to form final structure using RIE etching.

Figure 3-6 Schematic fabrication procedure of all-organic diodes

After that, PEDT/PSS or PPy about 1 μm thick was then deposited by spin coating. Then, the sample were cured at 120°C for 5 minutes and slowly cooled down to room temperature. Following that, both organic diodes were formed by the RIE technique. A layer of aluminum, 150 nm thick, was thermally evaporated as the metal pattern mask for the RIE etching. Upon patterning the Al, the RIE process was utilized to strip the photoresist and to etch the PEDT/PSS (or PPy) and NTCDA layers. Finally, the organic diodes were formed after the wet etching of Al layer. Figure 3-6 shows the detail fabrication procedure.

3.5 Results of Organic Diodes

Current-voltage measurements were performed on a Keithley SMU236 unit of the measurement setup shown in Figure 2-2 at room temperature. The measured current density versus voltage characteristics of NTCDA/PPy and NTCDA/(PEDT/PSS) diodes are illustrated in Figure 3-7 and Figure 3-8, respectively. Forward bias is defined here as positive voltage applied to the PPy or PEDT/PSS contact. From the experimental data, the rectification ratios can be found to be ~ 4.5×10^3 for NTCDA/PPy at 2 V and ~ 4.1×10^3 for NTCDA/(PEDT/PSS) at 3 V. The turn-on voltage of the NTCDA/(PEDT/PSS) diode is about 1.7 V, which is higher than that of the NTCDA/PPy diode, about 1.2 V. The NTCDA/(PEDT/PSS) diode has a lower current density at the forward bias compared to the NTCDA/PPy diode. The reason of the difference is attributed to the different material properties like bandgap and Fermi energy level.

The interface properties between the n-type organic material and the p-type organic material depend on the relative energies of the Fermi energy levels, the HOMO levels and the LUMO levels. Usually, the Fermi levels of the two materials align at the

interface. However, due to van der Waals' weak intermolecular bonding between organic semiconductors, the Fermi level would move freely at the organic interface and thus allowing the vacuum level to align [60]. The contact barrier would be determined by the ionization energy difference between two organic semiconductors. Here, the ionization energy is defined as the energy separation of the low binding energy edge of the HOMO from the vacuum level. From the reverse part of the curves in Figure 3-7 and Figure 3-8, the breakdown voltages for the NTCDA/PPy and NTCDA/(PEDT/PSS) are about 9 V and 8.3 V, respectively. Both of these kinds of organic diodes show the abrupt breakdown behavior.

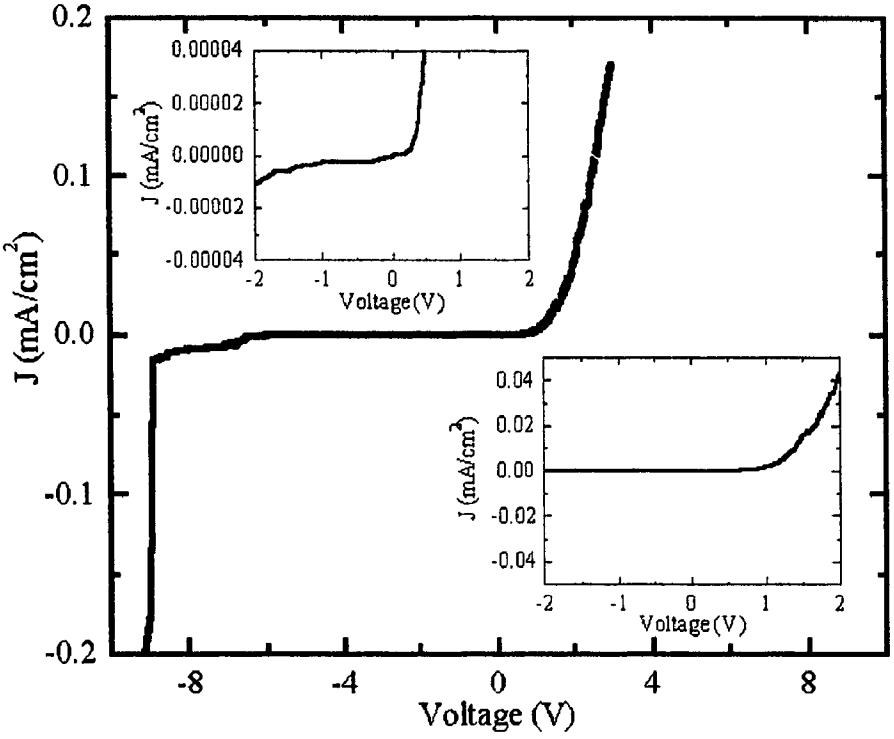


Figure 3-7 Current-voltage characteristics of NTCDA/PPy diode

The bandgap (Eg) of NTCDA is determined to be 3.3 eV from the absorption spectrum and its energetic distance between conduction band and Fermi level (E_C-E_F) is

less than 0.37 eV at 30°C [61]. The work function and the bandgap of PEDT are 5.16 eV [62] and about 1.6 eV [63], respectively. The difference between the conduction band's edge and vacuum level for PPy is 2.5 eV and the E_g is 3.16 eV. Its polaron level is about 5.19 eV relative to the vacuum level [64]. Thus, from the experiment barriers for these two diodes, the HOMO of NTCDA can be deduced to be about 6.9 eV from the vacuum level. Then, the LUMO of NTCDA will be 3.6 eV from the vacuum level.

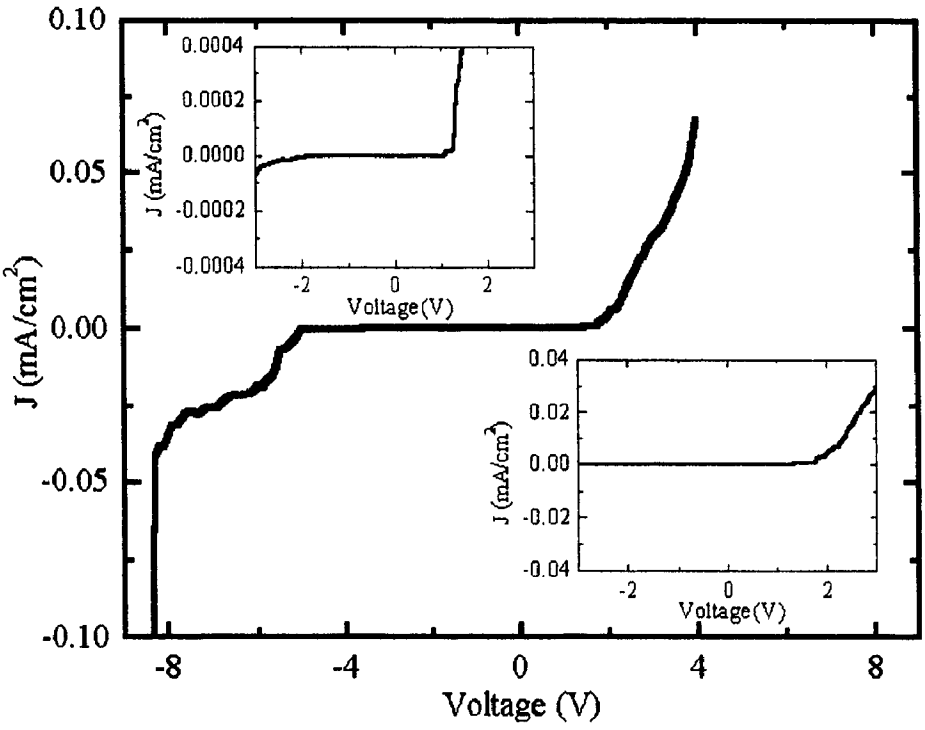


Figure 3-8 Current-voltage characteristics of NTCDA/(PEDT/PSS) diode

3.6 Acetone Treatment of NTCDA/PPy Organic Diodes

Acetone is a very common solution for photoresist removal in photolithographic process. However, acetone was found to significantly affect the electrical characteristics of diodes in this experiment. From the measured data of NTCDA/PPy diodes immersed

into an acetone solution for about 3 minutes, the significant change of I-V characteristics as shown in Figure 3-9 was observed due to the acetone attack.

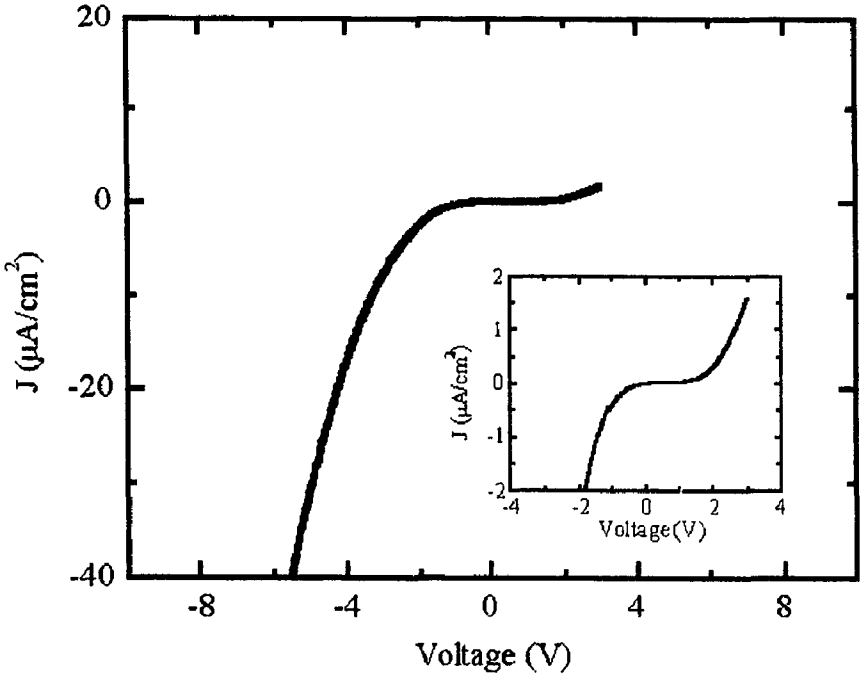


Figure 3-9 I-V characteristics of NTCDA/PPy after the acetone treatment

With acetone treatment, the current-voltage characteristics are found to be symmetric without abrupt breakdown behavior from Figure 3-9. The rectification ratio and the current density are dramatically decreased by three orders and the breakdown voltage is reduced to about one-third. This effect should be attributed to the strong influence of acetone on the conducting properties of PPy by changing the doping level. Thus, acetone should be avoided in the fabrication process of an NTCDA/PPy diode. As an alternative approach of patterning polymers, RIE process can be used to avoid the acetone attack because of its advantages such as clean and dry etching.

CHAPTER FOUR

PEDT/PSS FIELD-EFFECT TRANSISTORS

4.1 Introduction

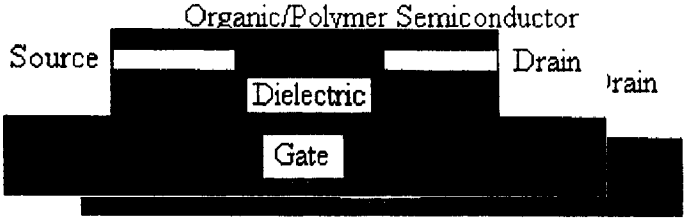
In this chapter, PEDT/PSS OFETs have been investigated and fabricated with the simple and low-cost fabrication processes of spin coating and RIE using PEDT/PSS as a p-type semiconductor, poly(4-Vinylphenol) (PVP) as a gate dielectric layer, PPy as source and drain electrodes, and PPy or heavily doped Si as the gate.

OFETs based on semiconductive polymers have attracted increasing interest for the promising applications to flexible, low-cost and large area displays, and low-end electronic devices like smart cards due to their extraordinary electrical and mechanical properties. A lot of undoped or doped conjugated polymer such as polyaniline [65], polythiophene [66], poly-3-hexyl-thiophene [67], arylamino-poly-(phenylene-vinylene) [68], and alpha-sexithiophene [69] have been demonstrated as the active materials for the OFETs. Since the organic FETs are generally used for low-cost applications, the easy fabrication processes and the simplified structures are of much interest.

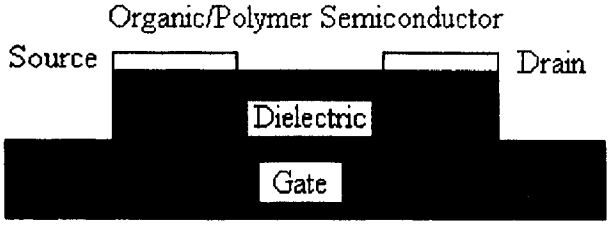
In this study, dielectric layer, semiconductor, gate and source/drain layer were deposited by the low-cost spin coating and then patterned with RIE technique using Aluminum thin-film as a mask. The electrical characteristics of the device and the influence of PPy on the device's performance have been investigated by comparing two

kinds of OFETs with different gate, PPy as the gate and low-resistivity silicon as the gate in the ambient atmosphere at room temperature.

4.2 Theory of OFETs



(a) Bottom contact.



(b) Top contact.

Figure 4-1 Schematic structure of OFETs

Generally, OFETs have two kinds of basic structures shown in Figure 4-1, bottom contact and top contact. To analyze the electrical characteristics of OFET, the MOS theory for the traditional Si FETs was assumed to be still held. Thus, similar to the conventional FETs, the drain current in the linear region and the saturation region can be commonly described by equation 4-1 and 4-2 [70]:

$$I_D = \frac{W\mu_{FET}C_i}{L}V_{DS}(V_{GS} - V_{th}) \qquad (4\text{-}1)$$

$$I_{Dsat} = \frac{W\mu_{FET}C_i}{2L}(V_{GS} - V_{th})^2 \qquad (4\text{-}2)$$

where W and L are the channel width and length, respectively, μ_{FET} is the carrier mobility of the holes in the PEDT/PSS channel, $C_i=\varepsilon_i/d_i$ is the gate dielectric capacitance per unit area (ε_i and d_i are the dielectric constant and the film thickness of the gate dielectric layer, respectively), and V_{GS}, V_{DS}, V_{th} are the gate voltage, drain-source voltage and threshold voltage, respectively.

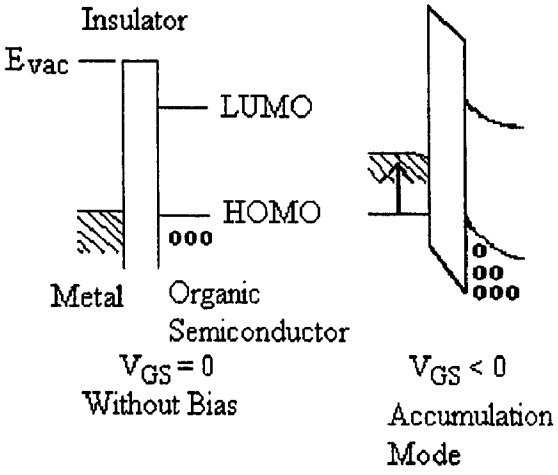


Figure 4-2 Schematic Band diagram of p-type OFET

The operation mode of OFETs is the accumulation mode or the depletion mode. For the p-type OFETs, in the depletion mode, OFETs are driven by a positive gate bias, resulting in high channel resistance (off-state). On the other hand, OFETs are driven by a negative gate bias in the accumulation mode, resulting in low channel resistance (on-state). Figure 4-2 shows a schematic energy diagram for the p-type OFETs under the state of without bias and accumulation mode.

4.3 Current-Voltage (I-V) Measurements

Current-voltage (I-V) measurements refer to d.c. characterization of OFETs for the purposes of performance analysis and parameter extraction. There are two sets of I-V

curves: drain characteristics and gate characteristics, which can be used to extract the important parameters of OFETs, such as the field-effect mobility (μ_{FET}), the threshold voltage (V_{th}), the slope, and the on/off current ratio.

4.3.1 Electrical Characteristics

Drain characteristics are a series of plots of the drain-source currents (I_D) as a function of drain-source voltage (V_{DS}) at different values of gate-source bias (V_{GS}). The plot consists of three regions: the linear region where V_{DS} is small compared to the sum of the gate's built-in potential, V_{bi} and V_{GS}, and the channel's current responds linearly to an increase in V_{DS} according to Equation 4-1; the cutoff region where the channel's current is restricted; and the saturation region where V_{DS} is sufficiently high to fully deplete the channel and I_D flow saturated at the saturation current, I_{DS}, from Equation 4-2.

Gate transfer characteristics are a plot of the I_D, as a function of V_{GS}, at specific value of V_{DS}. The field-effect mobility is one of the most important parameters of OFETs. It is often used to characterize the organic semiconductor of OFETs. The drain characteristics can be used to estimate the field-effect mobility, either from the saturation current or from the low drain current in linear region.

I_{on}/I_{off} ratio is also an important parameter of OFETs. It depends on the ratio of the mobility over conductivity, which simultaneously requires a large mobility and a low conductivity for the organic semiconductor to achieve a large on/off current ratio.

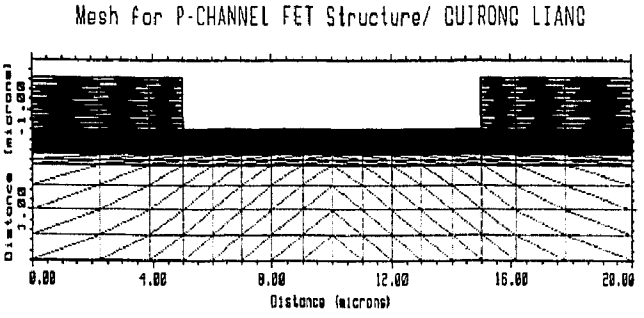
4.3.2 Measurement Set-up

The measurement set-up for electrical characterization of OFETs essentially consists of a probe station with a microscope, a Keithley Test System with ICS, and a personal computer (PC) as shown in Figure 2-2.

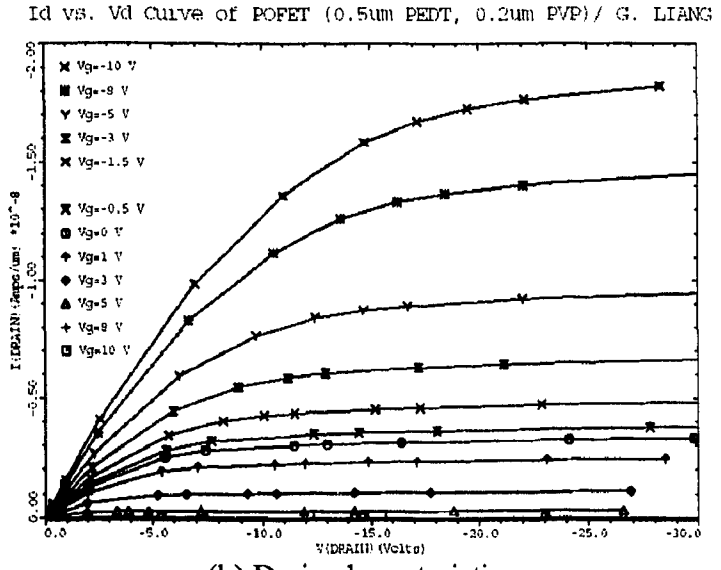
4.4 TCAD Simulation of OFETs

The purpose of Technology Computer Aided Design (TCAD) simulation of OFETs is to improve the device's performance by changing and optimizing the fabrication process conditions. With the help of TCAD simulation with TSUPREM-4 and MEDICI simulators, the fabrication conditions were optimized to obtain the better characteristics.

4.4.1 Simulation of OFETs

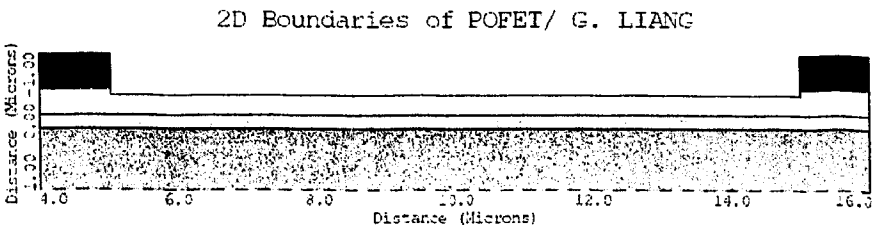


(a) Mesh of device.

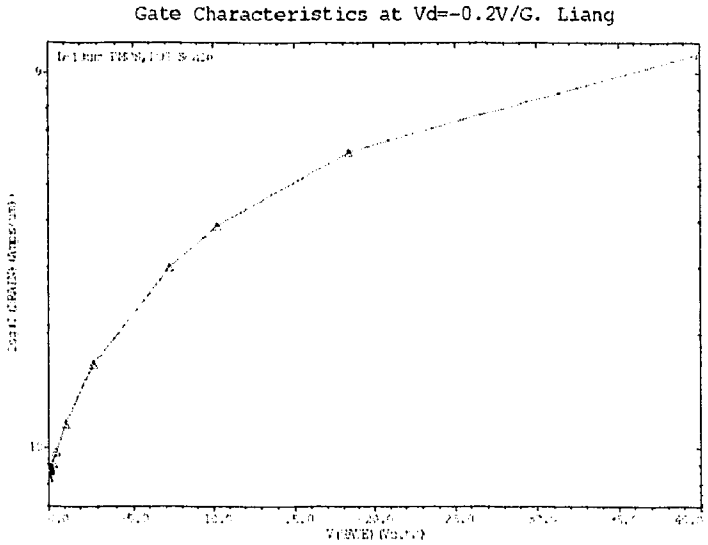


(b) Drain characteristics.

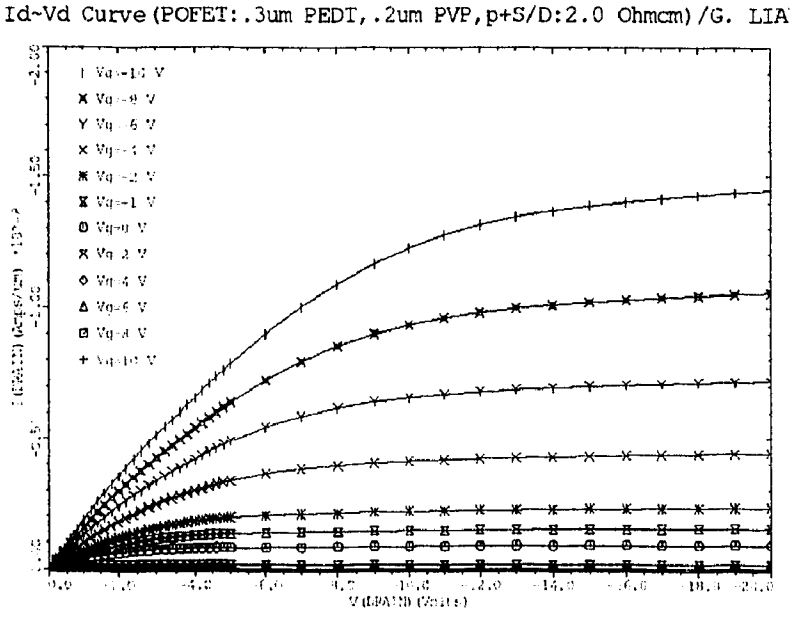
Figure 4-3 Mesh (a) and characteristics (b) of PEDT/PSS OFET with PVP



(a) Mesh structure.

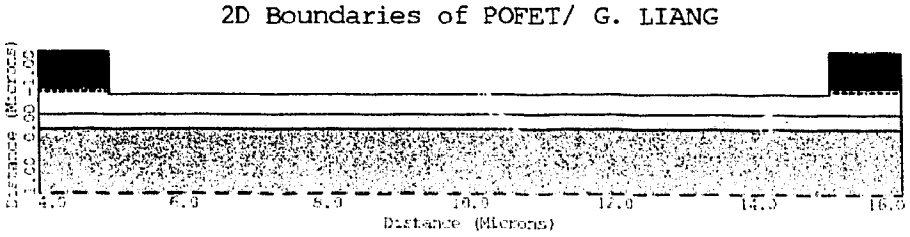


(b) Gate characteristics.

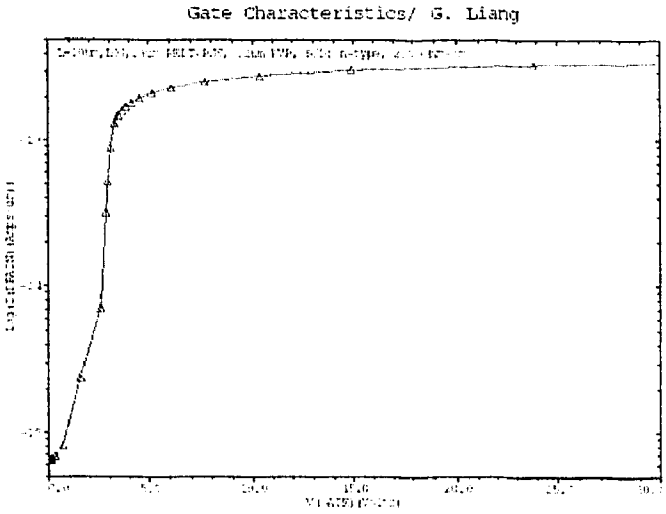


(c) Drain characteristics.

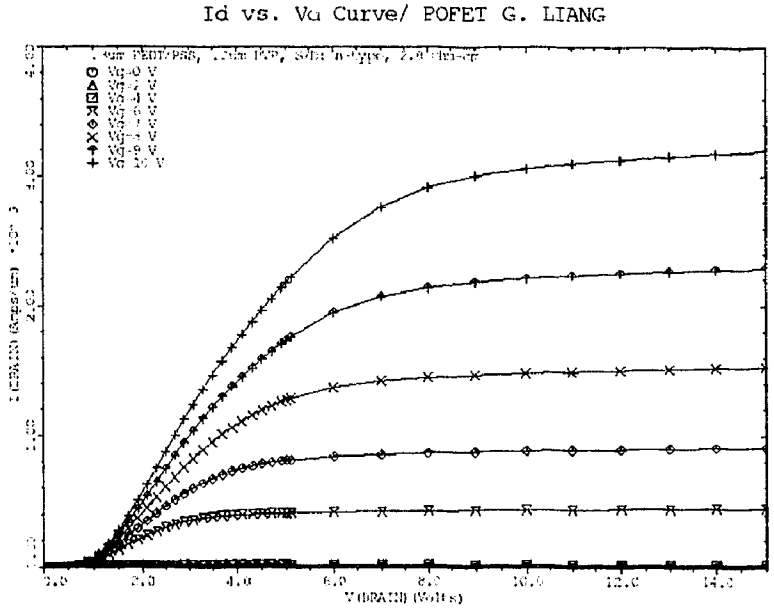
Figure 4-4 Mesh and Electrical Characteristics of OFET with p^+ Source/Drain



(a) Mesh structure.



(b) Gate characteristics.



(c) Drain characteristics.

Figure 4-5 Mesh and Electrical Characteristics of OFET with n^+ Source/Drain

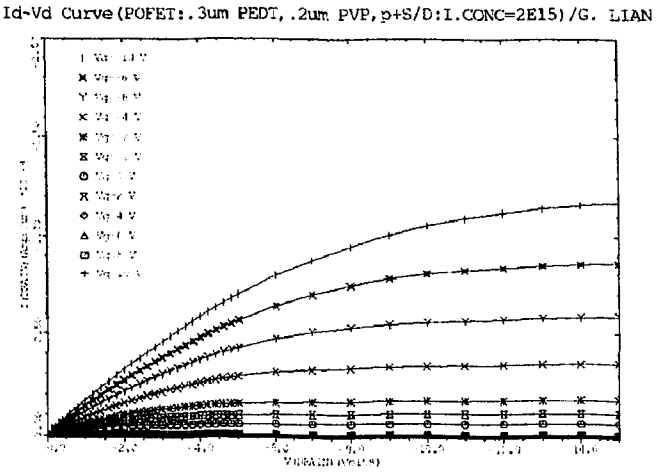


Figure 4-6 S/D: p-type, CONC=2e15; Channel: PEDT, CONC=1e16

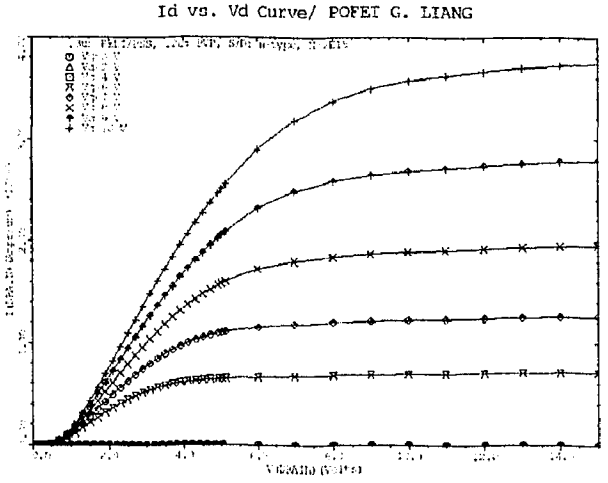


Figure 4-7 S/D: n-type, CONC=2e15; Channel: PEDT, CONC=1e16

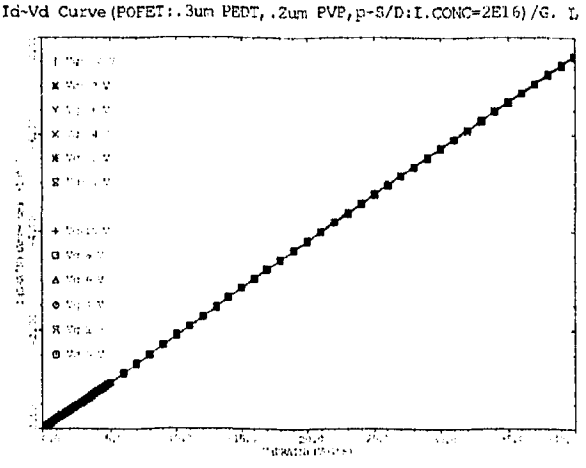


Figure 4-8 S/D: p-type, CONC=2e16; Channel: PEDT, CONC=1e19

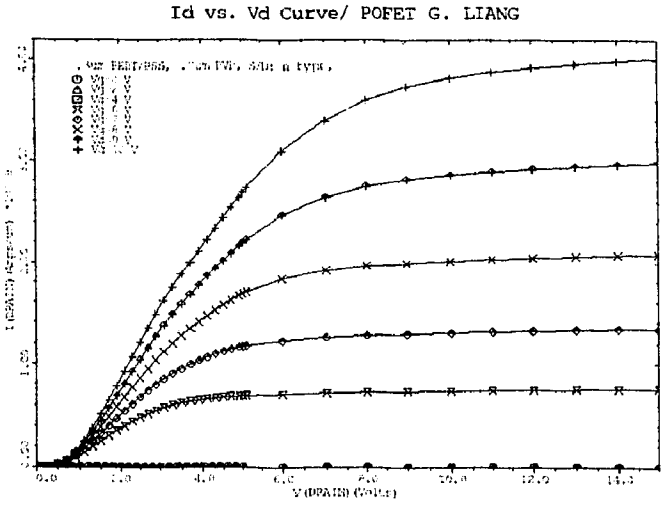


Figure 4-9 S/D: n-type, CONC=5e15; Channel: PEDT, CONC=1e16

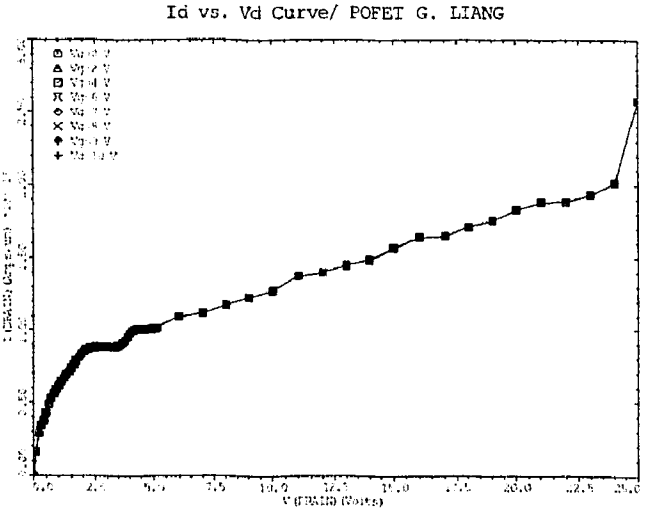


Figure 4-10 S/D: n-type, CONC=2e15; Channel: PEDT, CONC=1e18

In the simulation of polymer FET with TSUPREM-4 and MEDICI software, the mobility of Si was changed to 0.1 cm^2/VS and the resistivity of Si was changed to 1.26 Ωcm to represent the PEDT/PSS, a p-type polymer. PVP, a dielectric polymer, is represented by the silicon oxide. Because the constant mobility is used in the simulation, the mobility models that are independent on the dopant concentration were chosen.

The following two FET structures were simulated: one is with PVP of 500 nm thick and PEDT/PSS of 1 μm thick; the other one is with PVP of 200 nm thick and

PEDT/PSS of 0.5 μm thick. In the former structure, the V_{th} is about 9.881 V at V_{DS}=-0.5 V, and the slope is about 23 V/dec. For later one, V_{th} is 1.91 V at V_{DS}=-0.5 V, and the slope is 4.68 V/dec. Figure 4-3 shows the mesh structures and characteristics of later one.

4.4.2 OFETs with Different Source/Drain

In order to further investigate the influence on electrical characteristics of different device structures, OFETs with different types of Source/Drain materials were simulated: one with n^+ polymer and the other one with p^+ polymer. For both of these two FETs, they have the following main dimensions: 0.3 μm thick PEDT, 0.2 μm thick PVP, a channel length of 10 μm and a source/drain resistivity of 2 Ohm·cm.

With p^+ Source/Drain, OFET works under the accumulation mode with V_{th} of 1.544 V at V_{DS}=-0.2 V, and a slope of 3.742 V/dec. When V_{GS}=0V, there is the current flowing between the source and drain, which means it is a normal-on device. To turn off the device, we need to apply a positive gate bias. When the more negative V_{GS} is applied, the drain-source current, I_{DS}, will increase. Fig. 4-4 shows its mesh structure and characteristics. The drain characteristics show two regions: the linear region and the saturation region, which are similar to that of the conventional Si MOSFET.

With n^+ Source/Drain, OFET operates under the inversion mode with Vth of 2.716 V at V_{DS}=0.2 V, and a slope of 394 mV/dec at V_{GS}=2.7 V. Because the OFET used the n-type material as the source/drain electrodes, there will be the contact barrier between the p-type semiconductor and source/drain electrodes and an inversion layer should be formed between the source and drain electrodes to make the current going through the OFET by applying a positive gate voltage. At a zero gate bias condition, there will be no drain current flowing through the device. But for the OFET with p-

material as the source/drain, the drain current will flow through the OFET since there is a conduction channel between the source and the drain, even when the gate is at zero bias condition. Thus, compared with OFETs with p^+ S/D, OFETs with n^+ S/D have a smaller subthreshold slope, a smaller off current at V_{GS}=0 and a larger on/off current ratio. It is the normal-off device. It means, a positive V_{GS} larger than V_{th} should be applied to turn on the device by forming the conduction channel between the source and drain. The drain characteristics also show the linear region and the saturation region. Fig. 4-5 shows its mesh structure and characteristics.

4.4.3 OFETs with Various Doping Concentration

OFETs were simulated with changing the material's resistivity to related doping concentration. The similar results were obtained as those using resistivity in the TSUPREM-4 processing code. Fig. 4-6 and Fig. 4-7 show the resulted characteristics. While the doping concentration was increased over 1E17 cm^{-3}, such as 1E18 or 1E19, the V_{th} was to have more negative values, and the subthreshold slope was to be much larger, over 1e6 V/decade according the simulation output. Fig. 4-8 shows the drain characteristics of OFET with p-type S/D and a PEDT concentration of 1e19 cm^{-3}. Fig. 4-9 and Fig. 4-10 show the drain characteristics of OFET with n-type S/D and PEDT as the semiconductor. These should be contributed to the high channel doping concentration since the inversion channel is too hard to be formed.

4.4.4 Simulation Summary

Through the TCAD simulation with TSUPREM-4 and MEDICI simulator, simulation results of the different kinds of OFET structures can be summarized in Table 4-1. According to the above discussion and Table 4-1, it was found that OFET's

performances were strongly influenced by the PVP thickness, the semiconductor's (PEDT/PSS) thickness, and the types of S/D materials. The thinner the PVP and the PEDT/PSS, the better the performance. These may result from several reasons. First, when the thickness of a gate dielectric (PVP) and semiconductor (PEDT/PSS) were thinner, the electric field between the gate and the source/drain will be higher and then more charge carriers will be induced or attracted into the conduction channel with a smaller gate voltage. Second, the semiconductor's thickness will affect the off-current when the OFETs use the p-type material as the source/drain electrodes. The off-current will be smaller in cases of the thinner semiconductor. Third, when the OFETs use the n-type material as the source/drain, the conduction channel between the source and the drain was formed by an inversion layer. This will result in a very small drain-source current at the zero gate voltage.

Table 4-1 Summary of simulation results of the different OFET structures

	V_{th} (V)	Slope (V/Dec)	I_{off} (A/μm)	I_{on}/I_{off}	Working mode
P-type S/D (T_{PVP}=0.5μm, T_{PEDT}=1μm)	9.881	23	-1.7149E-10	small	accumulation mode/ normally-on
P-type S/D (T_{PVP}=0.2μm, T_{PEDT}=0.5μm)	1.91	4.68	-3.3987E-10	small	
P-type S/D (T_{PVP}=0.2μm, T_{PEDT}=0.3μm)	1.544	3.742	-8.2798E-11	medium	
N-type S/D (T_{PVP}=0.2μm, T_{PEDT}=0.5μm)	2.0	59	2.3E-16	small	inversion mode/ normally-off
N-type S/D (T_{PVP}=0.2μm, T_{PEDT}=0.3μm)	2.716	0.394	6.4525E-16	large	

From Table 4-1, we find the last OFET with n-type S/D will have the best electrical characteristics among all structures, with a small threshold voltage, a small subthreshold slope, and a large on/off current ratio. For the OFET with n-type polymer as the Source/Drain, the channel doping concentration cannot be too high to form the inversion layer for conduction channel. In conclusion, to improve an OFET's performance, it is necessary to decrease the thickness of the dielectric layer and the thickness of the semiconductor layer, and choose the n-type polymer conductor as the source/drain material.

4.5 Fabrication of PEDT/PSS OFETs

PEDT/PSS used in this work is a promising p-type sem conductive polymer for electronic applications due to its excellent electrical and optical properties, such as the solution processability, the stability, and the transparent property with light and dark blue colors after it is dried [71].

The schematic cross-section view of the fabricated FET is shown in Fig. 4-11. For the fabrication of PEDT/PSS FETs, an n-type heavily doped silicon wafer with a resistivity of about 0.01 Ω·cm was used as the substrate and the gate electrode for convenience. PVP as the gate dielectric layer was spun on the substrate after cleaning the wafer. The thickness of the PVP layer was 800 nm. Then the wafer was cured on the hot plate at 110°C for 5 minutes to remove the solvent from the thin film. After baking the PVP, the PEDT/PSS and the polypyrrole (PPy working as source/drain electrodes) were deposited by spin-coating in sequence. The sample was cured at 115°C for 5 minutes after each spin-coating. The measured thickness of the PEDT/PSS was 1 μm.

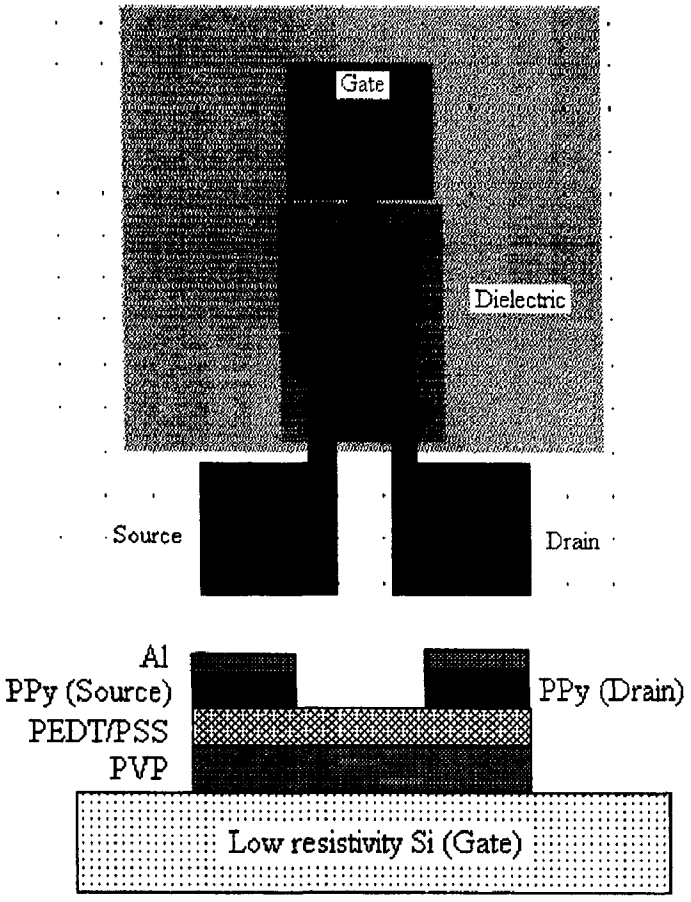
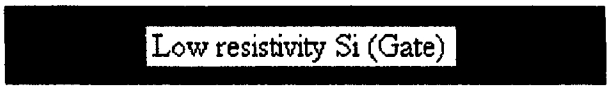
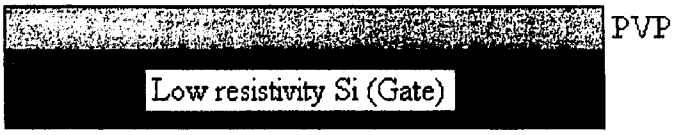


Figure 4-11 Mask (Top) and schematic structure (Bottom) of PEDT/PSS FETs

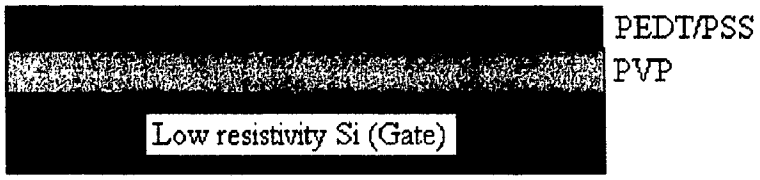
Here, a layer of aluminum, 120 nm thick, was thermally evaporated as the pattern mask for RIE process. In this work, two RIE steps were utilized to pattern the polymer layer. Finally, the PEDT/PSS FETs were implemented with the wet etching for aluminum layer and the RIE etching for polymer layers. The first aluminum wet etching and RIE are used to pattern the whole structure. The following Al wet etching forms the source and drain mask for a second RIE etching of PPy to obtain the final device as shown in Fig. 4-11. The detail fabrication procedure was described in Figure 4-12.



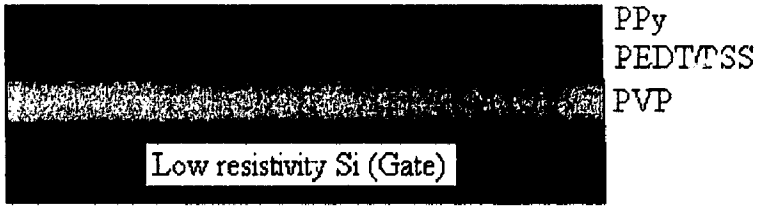
a. Prepare low-resistivity Si substrate as the gate;



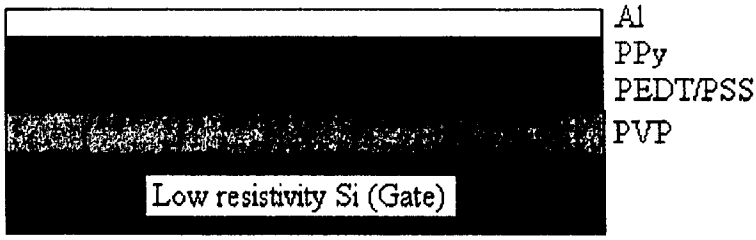
b. Spin-coat a layer of PVP as the gate dielectric;



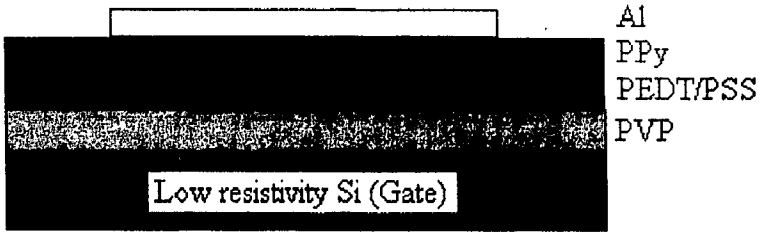
c. Spin-coat a layer of PEDT/PSS as the semiconductor;



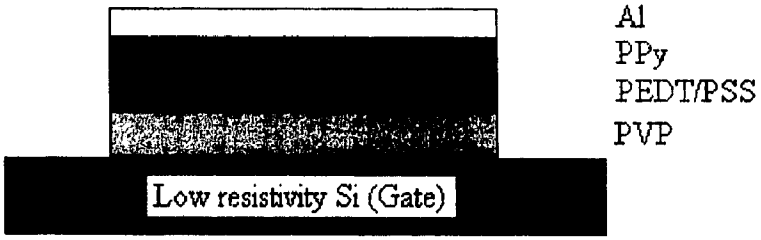
d. Spin-coat a layer of PPy as the Source/Drain electrode;



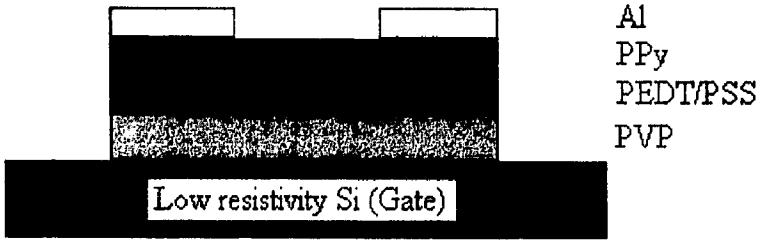
e. Evaporate a layer of Al as RIE metal mask;



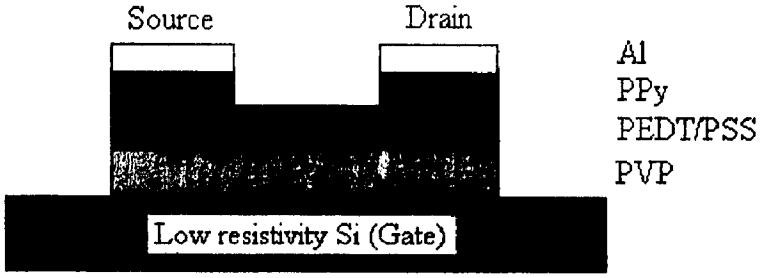
f. Pattern Al layer by wet-etching;



g. Pattern all polymer layers by RIE etching;



h. Pattern Al to form Source/Drain mask by wet-etching;



i. Pattern PPy above the channel to form S/D and final structure;

Figure 4-12 Schematic fabrication procedure of PEDT/PSS based OFETs

4.6 Results of PEDT/PSS OFETs

For the FET described above, the drain characteristics of a typical FET fabricated with the PEDT/PSS as a semiconductor and the PPy as the source and drain materials are shown in Fig. 4-13. This device has a channel length and width of 40 and 300 μm, respectively, and a gate dielectric thickness of 800 nm. In the polymer-based FETs, the I_D is controlled by the V_{GS} applied to the low-resistivity Si. The negative gate voltages enlarge the conduction channel due to the formation of the hole accumulation layer.

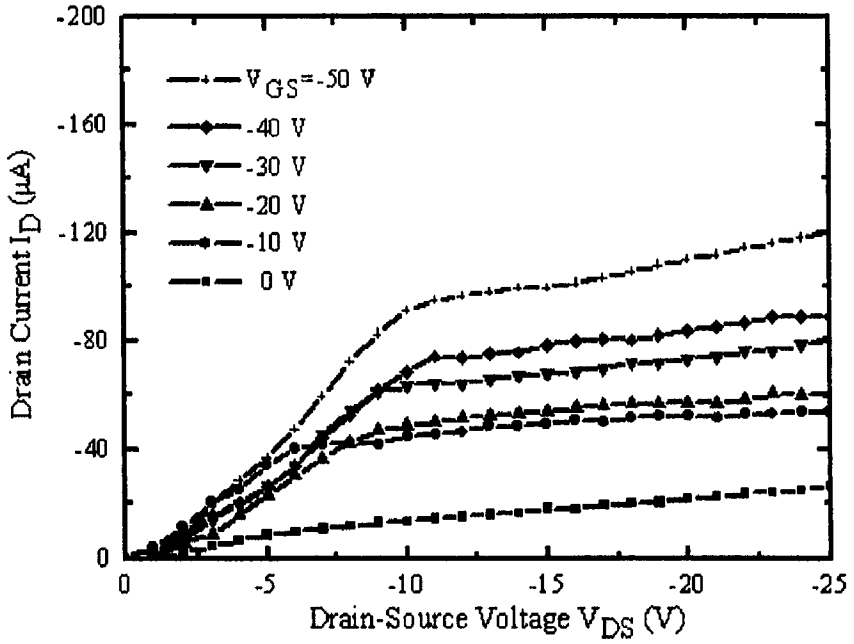


Figure 4-13 Drain characteristics of PEDT/PSS OFET with n^+ Si as gate

From Fig. 4-13, it is found when V_{GS} is at zero volts bias, the current between the drain and source, I_D increases linearly with the drain-source voltage, V_{DS}. However, when the applied V_{GS} is more negative, I_D rises more sharply at the small V_{DS} and shows a tendency to saturate at a relatively high drain-source voltage. Thus, the characteristics of FET have two working regions: linear region and saturated region, as shown in Fig. 4-13.

It indicates the channel's conductivity is increased with a negative gate voltage. From Fig. 4-13, it also shows that the PEDT/PSS works as a p-type organic semiconductor with the holes as the majority carriers. When a negative bias is applied to the gate electrode, the holes are attracted to the region near the dielectric layer between the drain and source. Under this bias condition, the conductivity of the channel between the drain and source is increased. Thus, the field-effect of this FET is due to the accumulation of the holes in the PEDT/PSS film near the PVP gate dielectric layer between the drain and source.

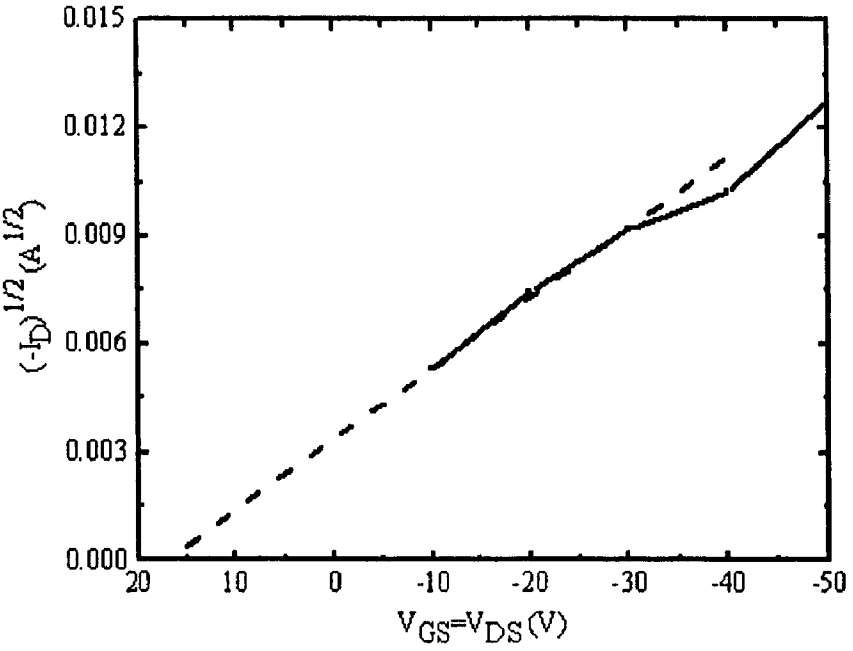


Figure 4-14 $I_D^{1/2}$ vs. V_{GS} of PEDT/PSS OFET with n^+ Si as gate

Fig. 4-14 shows the measured $I_D^{1/2}$ versus V_{GS} (=V_{DS}) characteristics of the PEDT/PSS based FETs, which can be used to extract the threshold voltage (V_{th}) according to the equation (4-2). By using the approach highlighted in the reference [65], the threshold voltage was extracted to be 17 V by extrapolating the linear part of the $I_D^{1/2}$ versus V_{GS} plot to the gate bias axis as shown in Figure 4-14. This value seems to be larger than what one may deduce from the results in Figure 4-13, and this may be

attributed to some error in the measured data used. This positive V_{th} indicates that the FET is a normally-on transistor with a conduction channel under the zero gate voltage. The hole mobility μ_{FET} can be calculated to be 0.8 $cm^2/V \cdot S$ from equation (4-2) and Fig. 4-14. To be useful, the organic FETs must have a sufficiently large on current and low off current for the practical applications. When the V_{DS} of –8 V is applied and the gate voltage is swept from 20 V to –50 V, the current on/off ratio is about 1.05×10^5 and the subthreshold slope is about 4.5 V/decade.

The charge transport in the semiconductive polymer is strongly affected by the doping concentration. The resistivity of the PEDT/PSS, as measured by Keithley 236 instrument using two parallel Au electrodes, was found to be 1.26 Ω·cm. Thus, from the equation $\sigma=q\mu p$ (q is the elementary electron charge), the carrier's concentration, p, can be found to be 6.2×10^{18} cm^{-3}, which are close to the doping concentration of PEDT/PSS.

4.7 Fabrication of All-Organic PEDT/PSS FETs

The schematic structure of a fabricated FET with PPy as the gate is shown in Fig. 4-15. To fabricate organic PEDT/PSS FETs, a silicon wafer coated with 0.5 μm thermally oxide was used as the substrate. After the wafer was cleaned, a polypyrrole of about 1 μm thick was spin-coated as the gate electrode and dried on the hot plate. Then, a PVP of 800 nm thick was also spin-coated as the gate dielectric layer. Then the wafer was cured on the hot plate at 110°C for 5 minutes to remove the solvent in the thin film. After baking the PVP, the PEDT/PSS and the conductive polymer polypyrrole were deposited by spin-coating and cured at 115°C for 5 minutes in sequence. The thickness of the PEDT/PSS and the top PPy layer are 1 μm and 500 nm, respectively.

In this experiment, two reactive ion etching steps were utilized to pattern the polymer layers. Here, a layer of aluminum 120 nm thick was thermally evaporated as the pattern mask for the RIE process. The first aluminum wet etching forms the RIE metal mask that covers the source, drain and channel regions. The following RIE etching is used to pattern the top PPy layer and PEDT/PSS layer. The second aluminum wet etching forms the source and drain mask for the second RIE etching of the top PPy layer in the channel region and the outside PVP layer. Because the RIE etching rate of PVP is higher than that of PPy, PVP on the outside region was etched away before the PPy in the channel region was completely etched. With a little reduction in the thickness of the bottom PPy layer, the final structure was formed when the top PPy layer in the channel region was completely removed. Figure 4-16 shows the detail fabrication procedure.

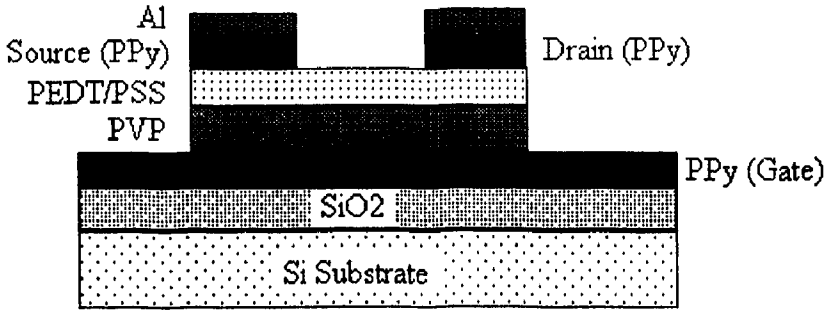
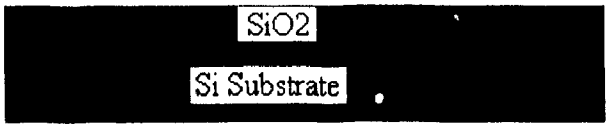
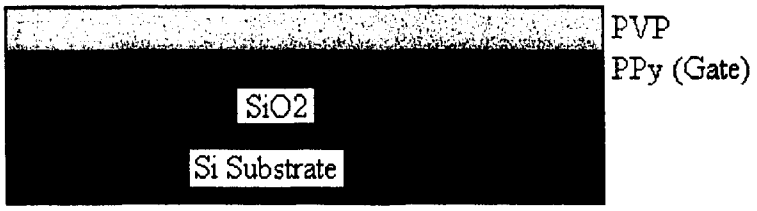


Figure 4-15 Schematic cross-sectional view of all-organic PEDT/PSS FETs

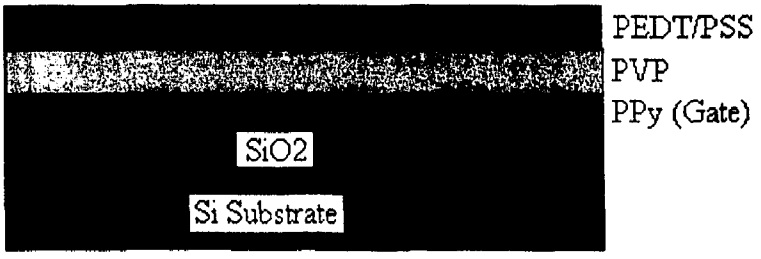


a. Prepare the SiO_2 coated silicon substrate;

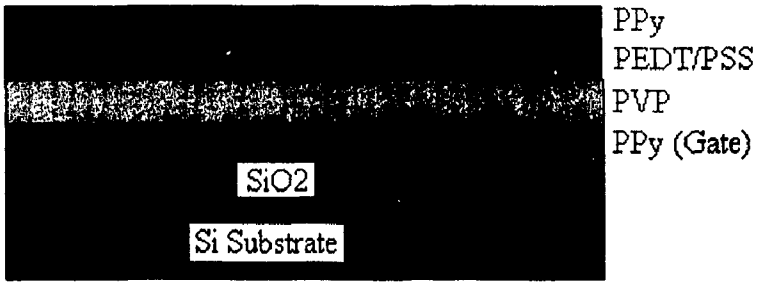
b. Spin a layer of PPy as the gate;



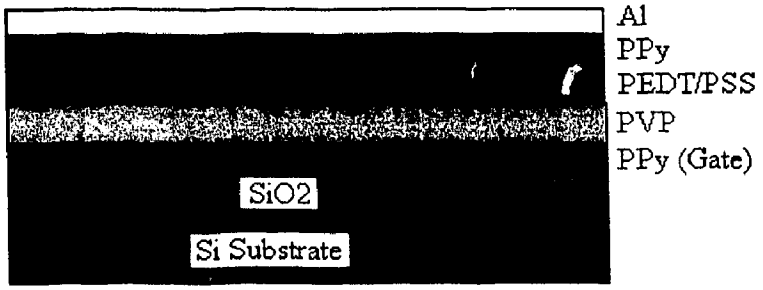
c. Spin-coat a layer of PVP as the gate dielectric;



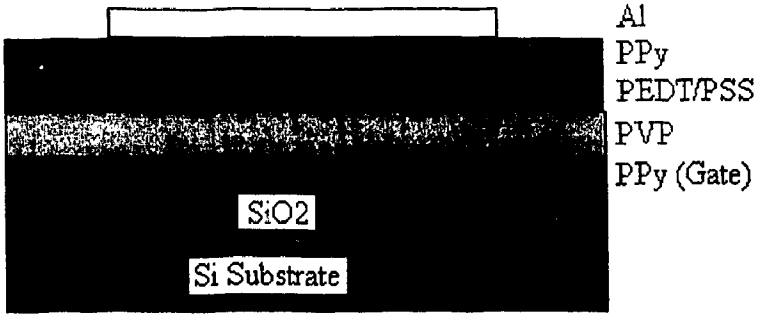
d. Spin-coat a layer of PEDT/PSS as the semiconductor;



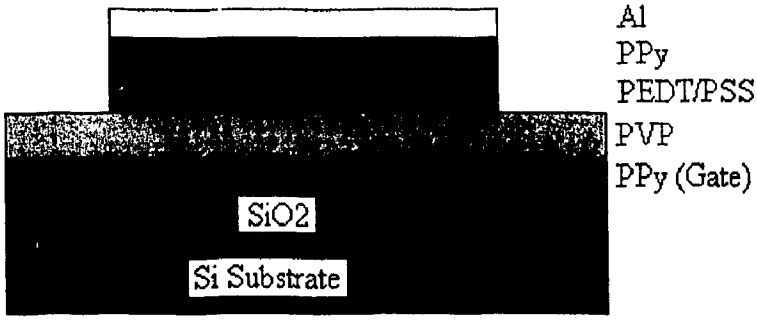
e. Spin-coat a layer of PPy as the Source/Drain electrode;



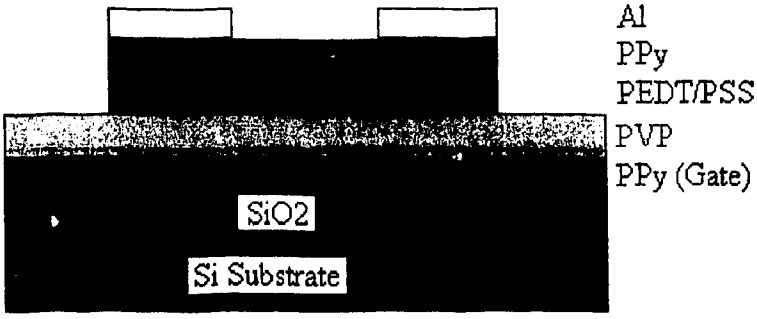
f. Evaporate a layer of Al as RIE metal mask;



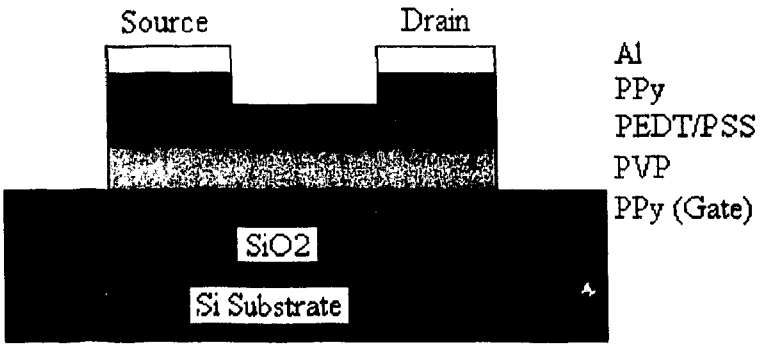
g. Pattern Al layer by wet-etching;



h. Pattern PPy and PEDT/PSS polymer layers by RIE etching;



i. Pattern Al to form Source/Drain mask by wet-etching;



j. Pattern PPy above channel and outside PVP to form S/D and final structure.

Figure 4-16 Schematic fabrication procedure of all-organic PEDT/PSS FETs

4.8 Results of All-Organic PEDT/PSS FETs

The I_D-V_{DS} drain characteristics of a typical all-organic FET fabricated with PEDT/PSS as the semiconductor and PPy as the source, drain and gate materials were shown in Fig. 4-17. This device has a channel length and width of 40 μm and 300 μm, respectively, and a gate dielectric layer 800 nm thick.

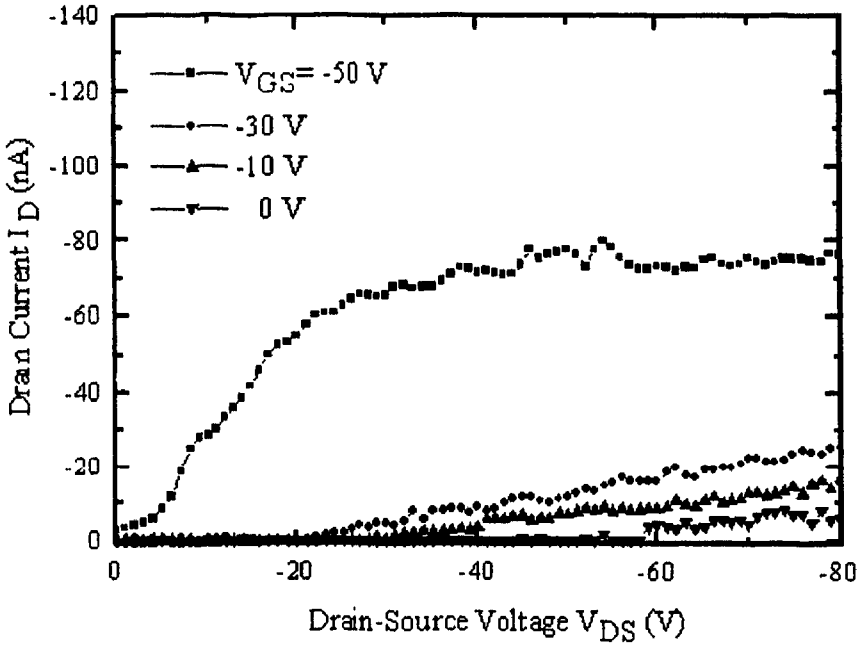


Figure 4-17 $I_D \sim V_{DS}$ curve of all-organic PEDT/PSS FET

Fig. 4-18 shows the measured gate transfer characteristics of the organic PEDT/PSS FET with PPy as the gate. The electrical characteristics were analyzed with the similar method stated above. By linearly extrapolating the curve to the V_{GS} axis, the threshold voltage V_{th} can be found to be -13.3 V. It implies the FET is a normally-off transistor. The hole mobility μ_{FET} in the linear region with the small V_{DS} of –15 V can be extracted to be 0.58×10^{-4} cm^2/Vs from the Fig. 4-18. When the V_{DS} of –15 V was applied and the gate voltage was swept from 20 V to –20 V, the slope was obtained to be about 6.77 V/decade.

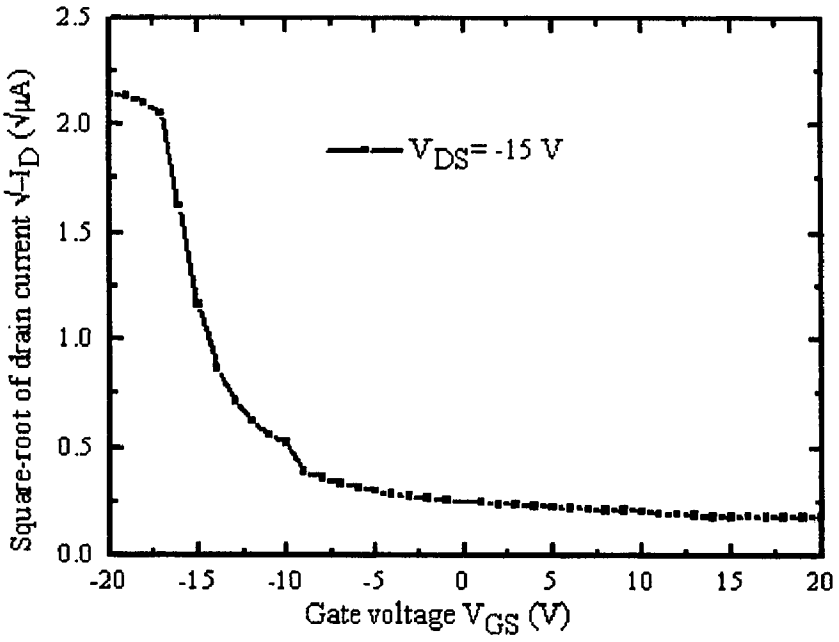


Figure 4-18 Gate transfer characteristics of all-organic PEDT/PSS FETs

By comparing their electrical characteristics of the above two OFETs with the same channel length and width under the same bias condition, it is found that the organic PEDT/PSS OFET with PPy as the gate has nearly a thousand times smaller drain current, smaller field-effect mobility, larger threshold voltage, and larger subthreshold slope than

the OFET with heavily doped silicon as the gate. The large differences observed between the two transistors should be attributed to the electrical properties of the gate material PPy and the dielectric material PVP. First, the different work function of PPy and n^+ doped Si will result in different band bending. Second, there is the leakage current flowing through the dielectric layer (PVP) during the measurement, which is on the order of 10^{-10} A. Thus, the effective electrical field of the applied gate voltage is decreased due to the smaller conductivity of PPy (generally less than 1 S/cm) compared to that of n^+ doped Si. Much less carriers will be attracted to form the conduction channel between drain and source. It means that the much larger gate voltage V_{GS} applied on the organic FET is necessary to achieve the drain current in the same order due to the largely weakened field effect.

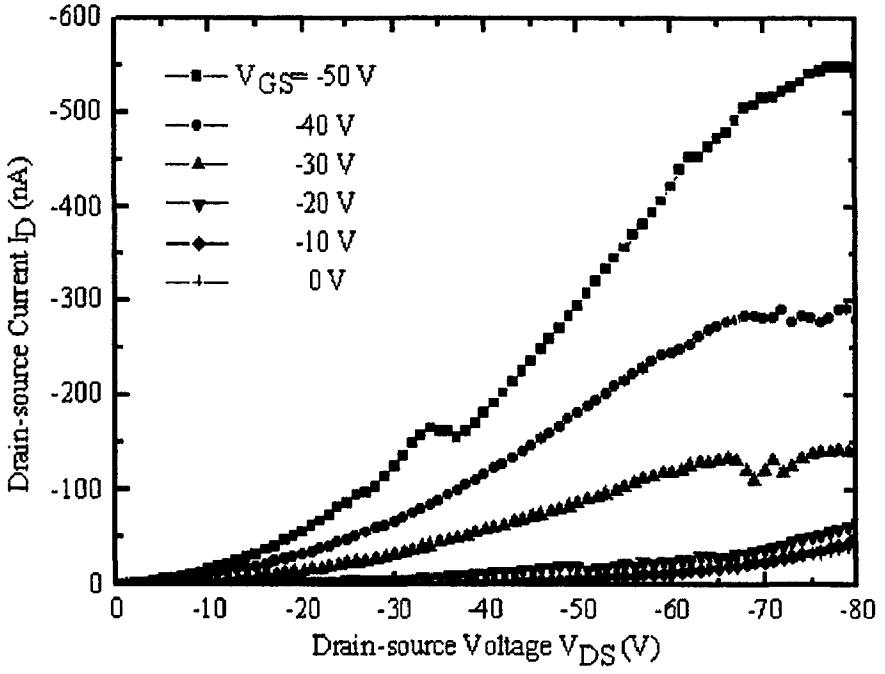


Figure 4-19 Drain characteristics of improved all-organic PEDT/PSS FET

For the practical applications, OFETs also need the smaller threshold voltage. Therefore, PPy functioning as the gate material strongly affects the electrical characteristics of OFET. To improve the performance and to benefit from the various advantages of organic FETs, we need to look for the conductive polymer with higher conductivity to work as the electrodes and other solution processable dielectric material to reduce the leakiness.

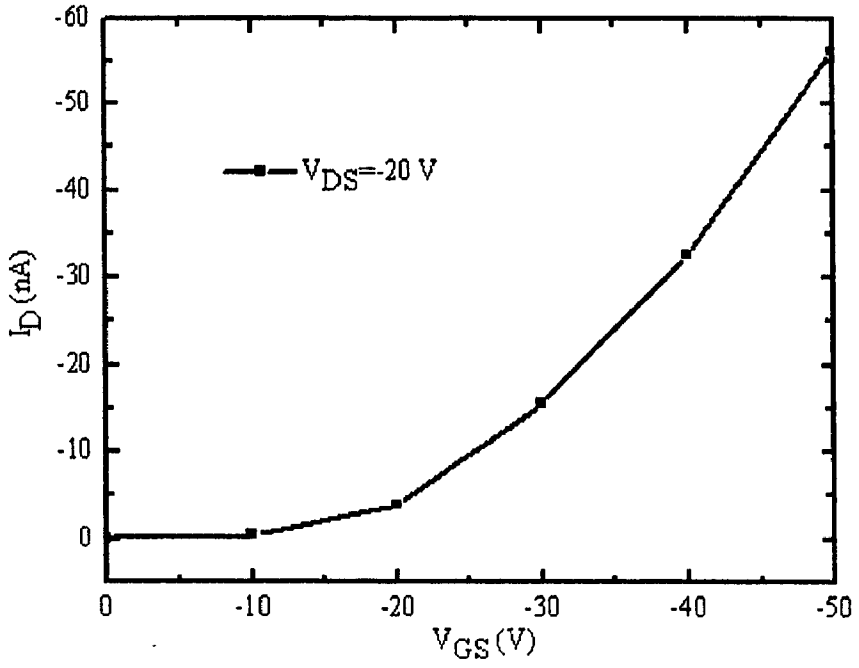


Figure 4-20 Gate characteristics of improved all-organic PEDT/PSS FET

From the above result of all-organic FETs, we can see the field-effect mobility is quite low with the value of 0.58×10^{-4} cm^2/Vs compared to the mobility of OFET with low-resistivity Si as the gate. This large difference of mobility extracted from the OFETs might result from the surface roughness of the gate dielectric. Because the surface of the low resistivity silicon wafer is much smoother than the surface of deposited conducting polymer (PPy), the surface of the gate dielectric (PVP) that was deposited on the low

resistivity silicon will be much smoother than the surface of PVP deposited on the PPy. And the rougher gate dielectric surface will reduce the field-effect mobility. Other reasons might include the electrical properties of the gate material PPy and the dielectric material PVP, such as the work function, the conductivity of PPy, and the gate series resistance effect. Moreover, according to the simulation of MOSFETs in section 4.3, we can find the performance of OFET could be affected by the thickness of the semiconductor and the gate dielectric. Therefore, the device's structure was modified by reducing the PEDT film's thickness to 600 nm and the thickness of PVP to 450 nm. Figure 4-19 and Figure 4-20 show the electrical characteristics of modified all-organic PEDT FETs with a channel length of 20 μm and a channel width of 300 μm. From these two figures, the field-effect mobility can be extracted to be 1.04×10^{-3} cm^2/Vs in the linear region with a small V_{DS} of –20 V, and a V_{th} of -16.8 V, a Slope of 10 V/dec, respectively. Here, we can find the field-effect mobility is improved by more than one order.

Since all polymer materials were deposited by spin coating and etched by RIE etching, the described fabrication processes may be a potentially low-cost method to fabricate the all-organic FETs and circuits for practical application with other polymers.

From the simulation results and the experimental results, it was found that the thickness of the organic semiconductor and gate dielectric have influence on the device's performance. The simulation is useful to improve the device's performance by optimizing the process. However, the charge mobility in the organic semiconductor is not constant and will be affected by the electric field and the temperature. Thus, the physically accurate mobility model should be selected in simulation.

CHAPTER FIVE

PENTACENE OFETS AND CIRCUITS

5.1 Pentacene OFETs and Stability

5.1.1 Introduction

From the experimental results of PEDT/PSS OFETs described in Chapter 4, we can observe that their operating voltage is very high and the electrical characteristics were not as good as those of Si based FETs. Pentacene, a promising p-type organic semiconductor consisting of five fused benzene rings with the chemical structure shown in Figure 5-1(a), has been investigated extensively as an active material for the devices since the 1990s. With improving process condition, it was observed to be one of the best candidates for electronic devices because of its increasing mobility. In this section, pentacene OFETs were fabricated with a simplified structure as shown in Figure 5-1(b). The stability of pentacene OFETs was investigated through the degradation with time.

5.1.2 Experimental

To fabricate the pentacene structure, n^+ heavily doped silicon was used as the gate electrode and the substrate. First, the top layer of the silicon wafer was thermally oxidized to form a 100 nm thick SiO_2 layer. Upon finishing the oxidation, a layer of gold, 80 nm thick, was deposited by the sputtering system. Then, photolithography was used to pattern Au layer as the source and drain electrodes. Pentacene, without further

purification, was thermally evaporated onto the sample held at room temperature to form the active thin-film with the low deposition rate and working pressure of 6×10^{-7} Torr. The photo image in Figure 5-2 shows the top view of the fabricated pentacene FET. The electrical characteristics were measured with Keithley SMU236 and 238 source measurement units in the ambient atmosphere at room temperature.

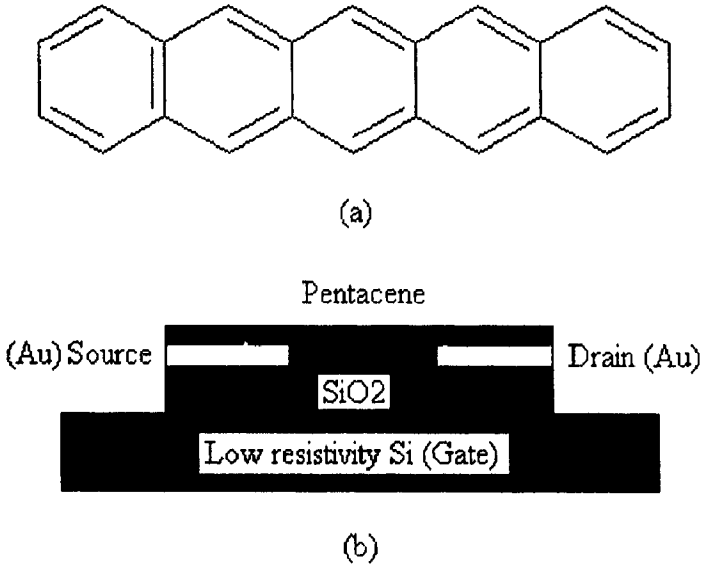


Figure 5-1 (a) Pentacene molecular; (b) Schematic structure of pentacene OFETs

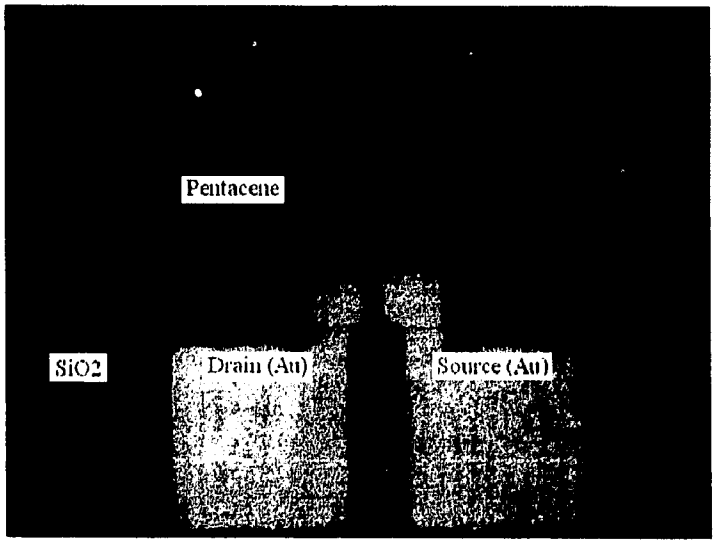


Figure 5-2 Photo image of top view of fabricated pentacene FET

5.1.3 Electrical Characteristics and Stability

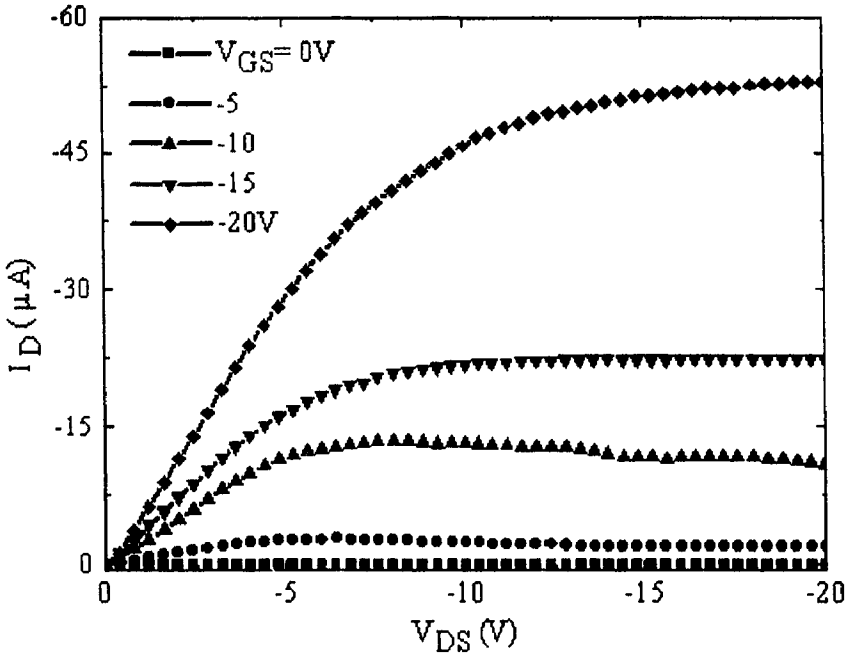


Figure 5-3 Drain characteristics of pentacene FET with thermal oxide as insulator

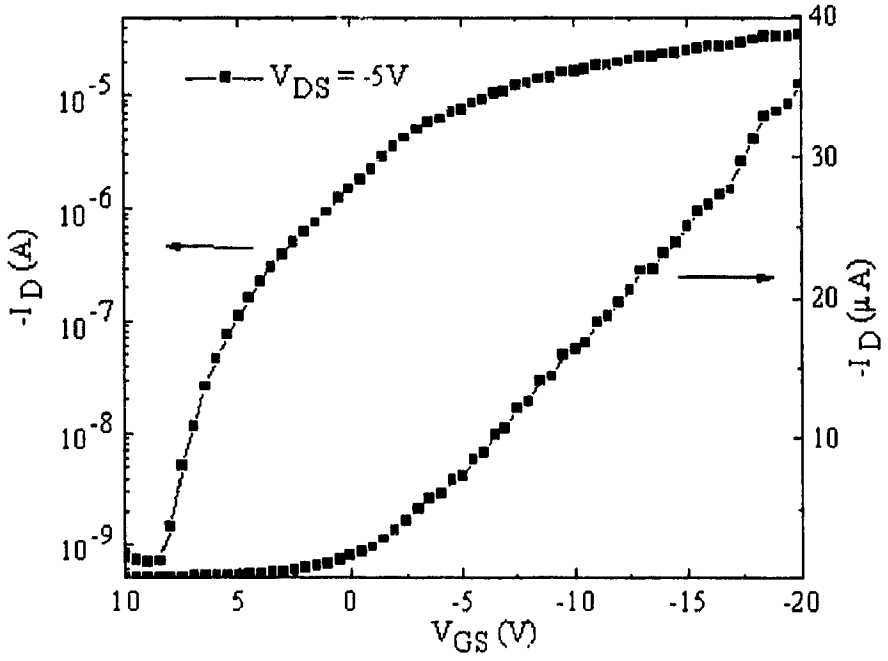


Figure 5-4 Gate characteristics of pentacene FET with thermal oxide as insulator

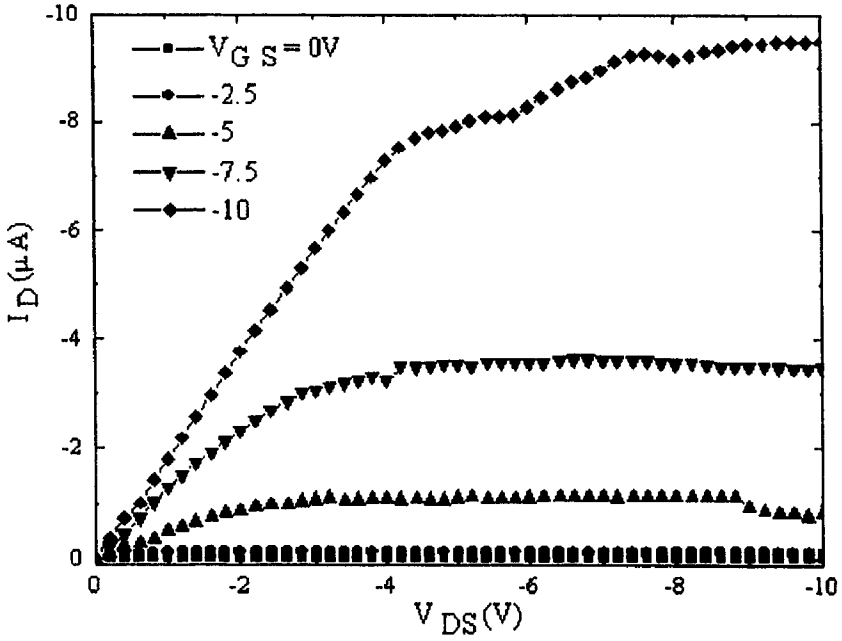


Figure 5-5 Drain characteristics of pentacene FET after one day

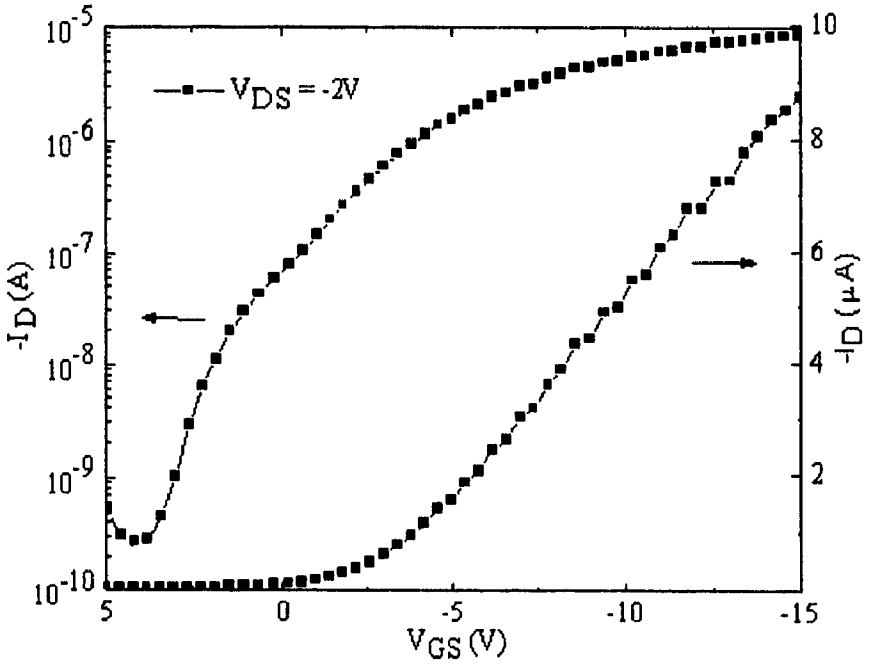


Figure 5-6 Gate characteristics of pentacene FET after one day

I_D-V_{DS} drain characteristics measured right after the fabrication of a typical pentacene FET were shown in Figure 5-3. This device has a channel length and width of 25 and 800 μm, respectively, and a gate dielectric thickness of 100 nm. Figure 5-4 shows the gate characteristics for this device. Based on the theory and equations described in Chapter 4, by using the similar approach, the main parameters of this device can be extracted as: a threshold voltage (V_{th}) of −1 V, a field-effect mobility (μ_{FET}) of 0.341 cm^2/Vs, an on/off current ratio (I_{on}/I_{off}) of 5.04×10^4, and a slope of 2.1 V/decade.

To investigate the stability of the pentacene OFETs, the electrical characteristics of fabricated OFETs were measured with the change of time, while the fabricated device was kept in the atmosphere environment. Figure 5-5 and Figure 5-6 show the electrical characteristics measured after one day, and the device's characteristics after one week were shown in Figure 5-7 and Figure 5-8. When the pentacene OFET was measured after one month, its electrical characteristics were shown in Figure 5-9 and Figure 5-10.

Table 5-1 shows the extracted main parameters of pentacene OFET after the fabrication, one day, one week, and one month. From Figure 5-2 to Figure 5-9 and Table 5-1, the degradation of the fabricated pentacene OFET was observed with the change of time. The field-effect mobility was reduced to 10 percent one week after the fabrication, and the magnitude of the on/off current ratio was decreased with one order. The threshold voltage and the slope increase with the extension of the device's lifetime.

The stability of fabricated pentacene OFET was not studied systematically, but all of these indicate that the pentacene OFET will degrade with the time if it is kept in the atmosphere environment without any measure of protection. The degradation might come from the interaction of pentacene material and the air. Thus, some protection methods

should be developed. For example, a layer of insulator like poly-methyl-meth-acrylate (PMMA) could be deposited to keep the pentacene from exposure to the air.

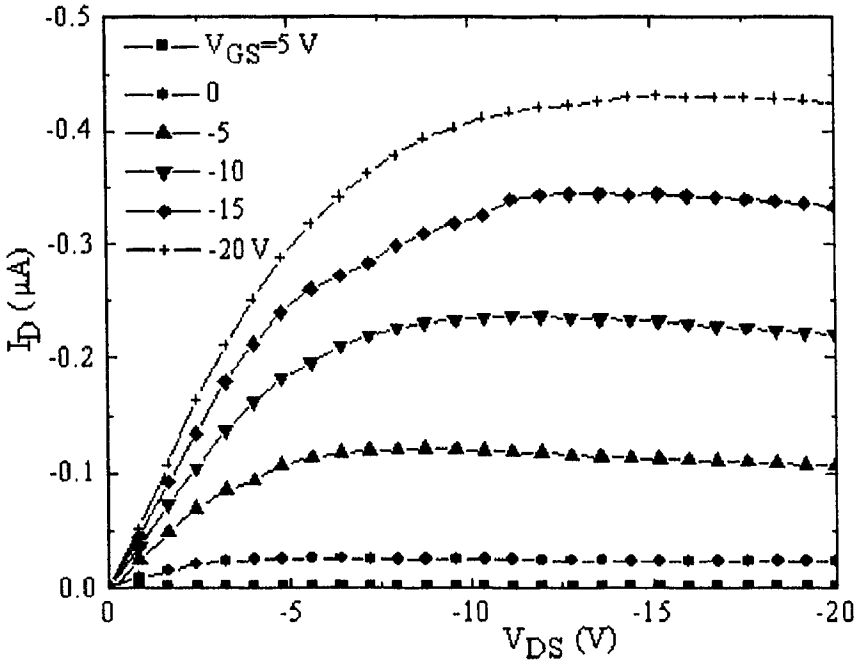


Figure 5-7 Drain characteristics of pentacene FET after one week

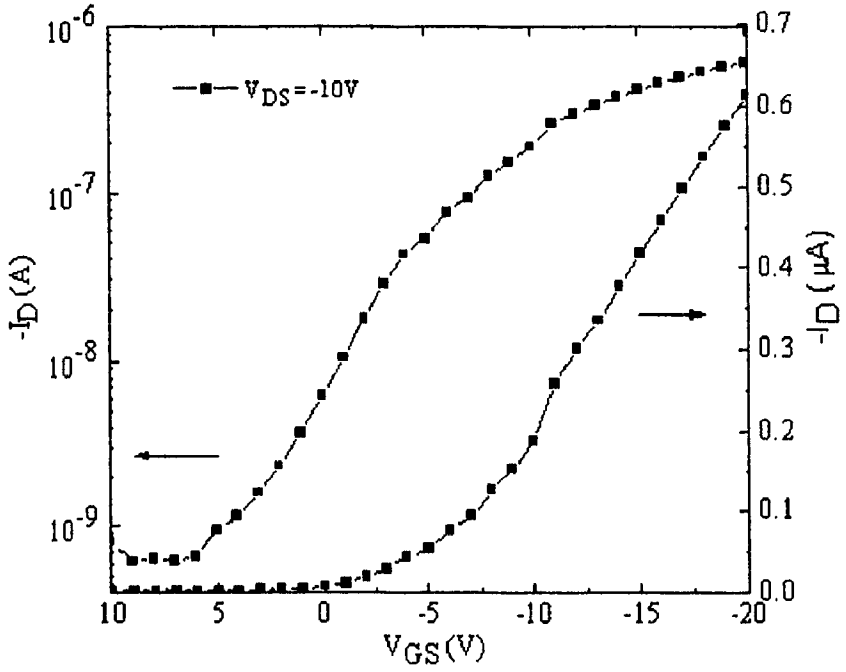


Figure 5-8 Gate characteristics of pentacene FET after one week

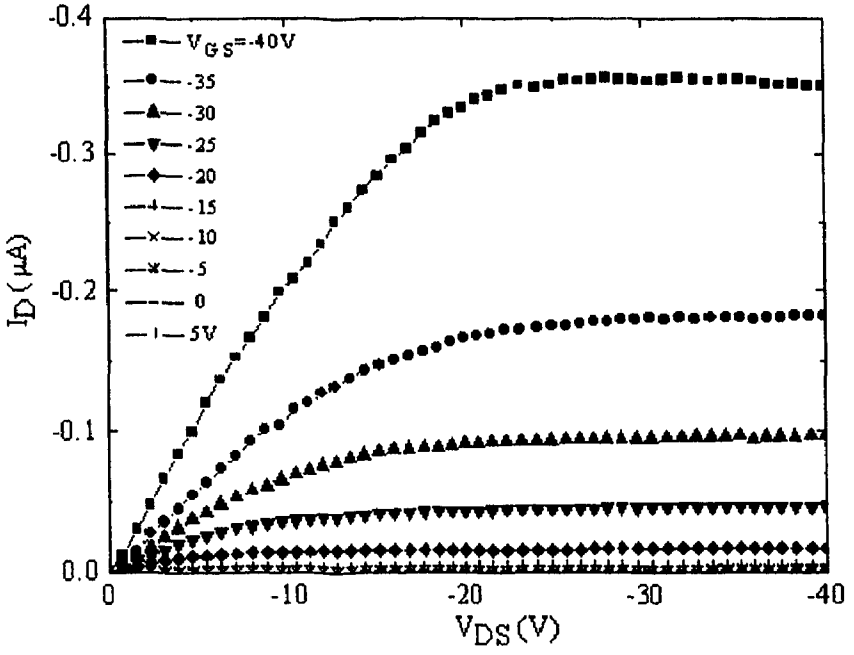


Figure 5-9 Drain characteristics of pentacene FET after one month

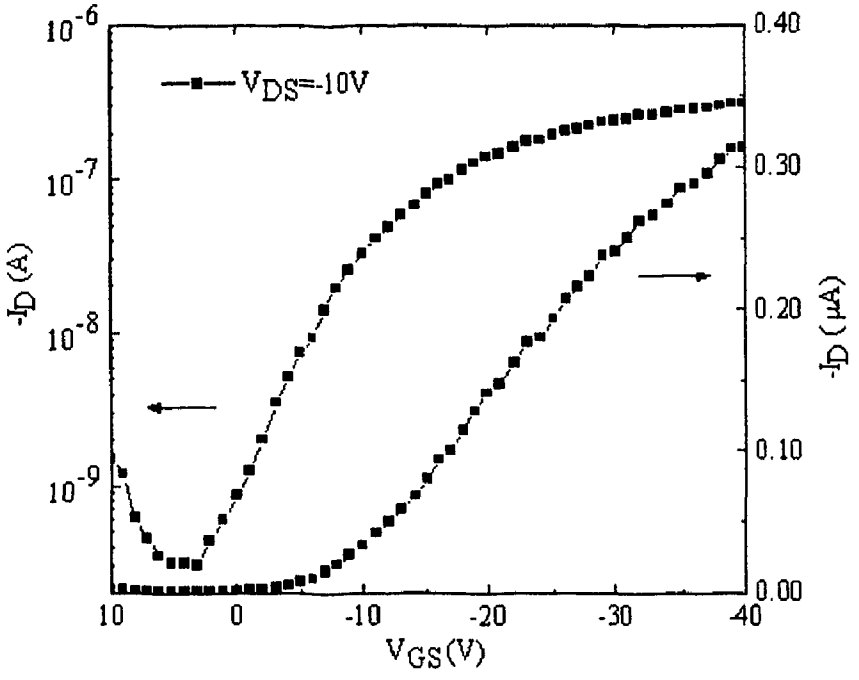


Figure 5-10 Gate characteristics of pentacene FET after one month

Table 5-1 Main parameters of pentacene OFET in different time

	μ_{FET} (cm^2/vs)	V_{th} (V)	Slope (V/Dec)	I_{on}/I_{off}
After fabrication	0.341	-1	2.1	5.04×10^4
One day later	0.315	-3	2.4	3.16×10^4
One week later	0.031	-4.2	4.5	1.0×10^3
One month later	0.01	-5.5	6.0	1.03×10^3

5.2 Temperature-Dependence of Mobility and V_{th}

5.2.1 Introduction

To gain insight and an understanding of the charge transport mechanism, here the temperature-dependence of field-effect mobility for pentacene OFET was observed. An increasing mobility with decreasing temperature has been reported in pentacene, indicating a band-like conduction [72]. In a field-effect transistor, the electrical conduction takes place at the semiconductor/gate dielectric interface, involving only the first several layers of a deposited semiconductor film. Thus, the orientation of the initial pentacene layer, surface properties of the insulator, and the substrate temperature should have a dominating influence on the field-effect mobility.

5.2.2 Experimental

100 nm-thick layer of SiO_2 is grown on n^+ heavily doped Si (Gate) wafer by thermal oxidation as the dielectric material. Then Au is deposited by sputtering. After that, two photolithography processes are performed to pattern Au as the source and drain and to pattern SiO_2, respectively. At last, pentacene (from Aldrich) is deposited on the channel (25 μm length and 800 μm width) and source/drain regions through a thermal evaporator at 6×10^{-7} Torr. The fabricated devices were tested by Keithley Test System (236 source measure unit with model H1001 heat control module) at an ambient

atmosphere. The electrical characteristics of pentacene FET are measured with sweeping temperature from 300 K to 400 K and then sweeping back.

5.2.3 Result and Discussion

The output and transfer characteristics of pentacene FET at room temperature were shown in Fig. 5-11 and Fig. 5-12, respectively. According to the equations described in Chapter 4, the electrical characteristics of the pentacene OFET were analyzed, and the field-effect mobility in saturation region was extracted to be 4.6×10^{-3} cm^2/Vs. Other parameters of pentacene FET can be extracted with a V_{th} of -4 V, a slope of 4.5 V/decade, and an on/off current ratio of 2×10^3. We can find even in cases where the sample preparation conditions were held the same as possible, large differences in mobility were observed compared to the extracted mobility (0.341 cm^2/Vs) in the previous section, which may ascribe to differences in purity of the pentacene material, thin-film deposition rate, molecular order, and grain boundary effects [73][74][75].

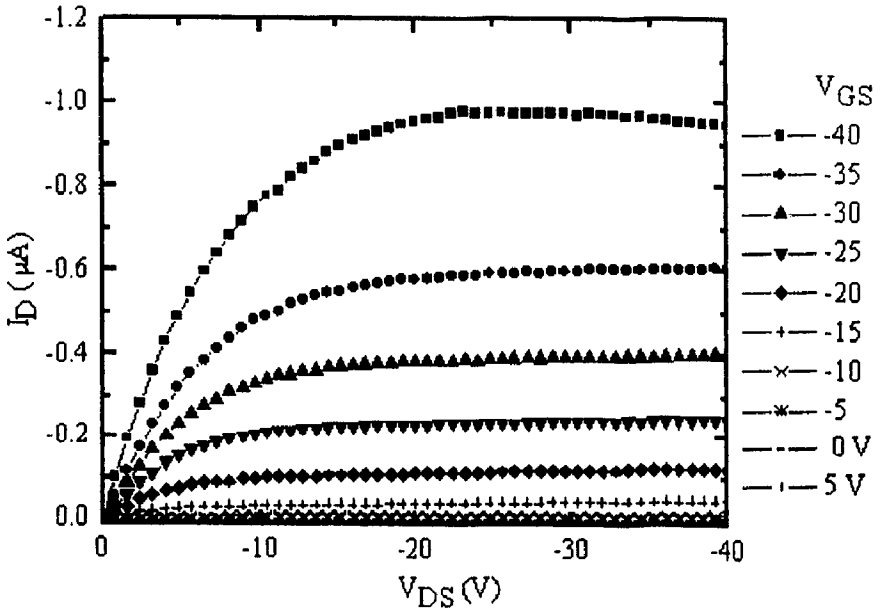


Figure 5-11 Drain characteristics of pentacene FET with thermal oxide as insulator

Mobility is the key parameter in FET and the extracted plot of mobility versus temperature is shown in Fig. 5-13. It could be found that the mobility increases to a peak and then decreases gradually to a very low value from 300 K to 400 K. Early experiments and analyses testify the thermally activated hopping transport for some organic materials below room temperature [76][77]. N. Karl [78] employed the inverse power law for this kind of temperature dependence in naphthalene crystal. In other words, mobility increases with the temperature (below room temperature) according to Arrhenius relations. But with the further increasing of temperature, the mobility in pentacene decreases eventually. This indicates the higher carrier scattering from higher carrier concentration at higher temperature.

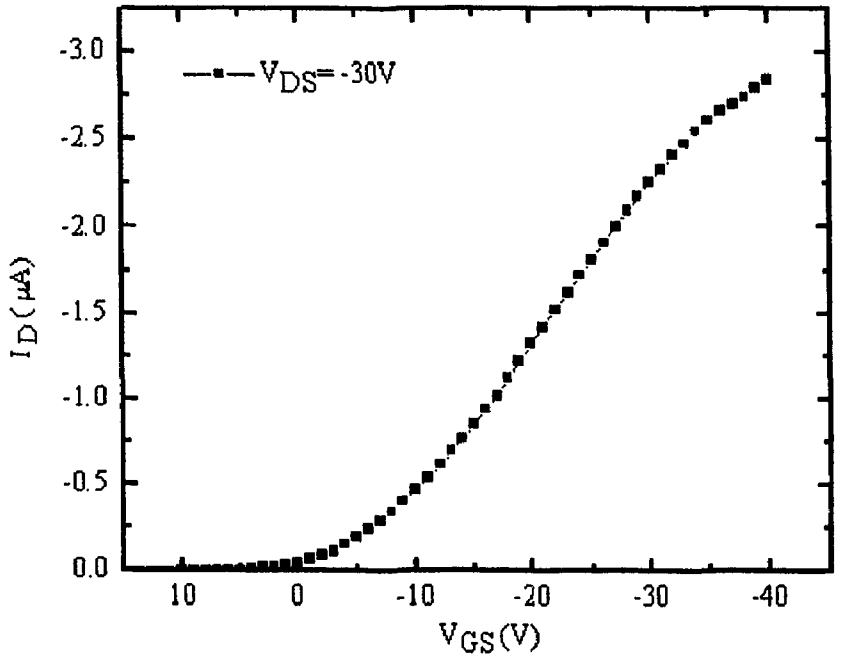


Figure 5-12 Gate characteristics of pentacene FET with thermal oxide as insulator

For the fabricated pentacene devices, mobility corresponding to temperature can be expressed by $\mu \alpha T^{-n}$ with n equal to -6 for 300 K – 330 K and 16 for 330 K – 400 K,

plotted in Fig. 5-14. Non-uniformity of n value suggests that other factors determine the mobility such as contact series resistance and electric field as well as temperature. After 330 K, the mobility decreases with the increasing of the temperature.

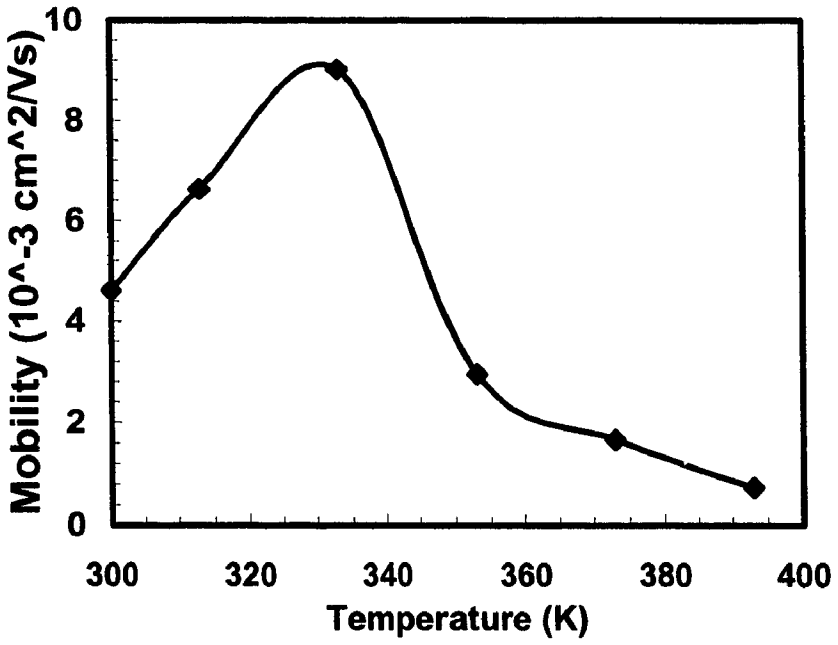


Figure 5-13 Temperature dependent mobility of pentacene FET

The mobility tail for temperature of 350 ~ 400 K may indicate the small polaron carrier generation and multiple traps in the pentacene film according to the model (Equation 1-1) developed by Holstein [15] and the multiple trapping and release (MTR) model (Equation 1-3) [16] developed by the Thiais group. When we sweep back the temperature and test the device again, the characteristics are almost the same, which demonstrates that there are no apparent annealing effects.

In this study, it was found that the threshold voltage of the fabricated pentacene FET is temperature dependent, as shown in Figure 5-15. From this figure, there is a minimum value of threshold voltage of about –1.4 V near 325 K. As the temperature

increases, the threshold voltage increases with almost a power law. It may be contributed to the higher carrier generated at a higher temperature.

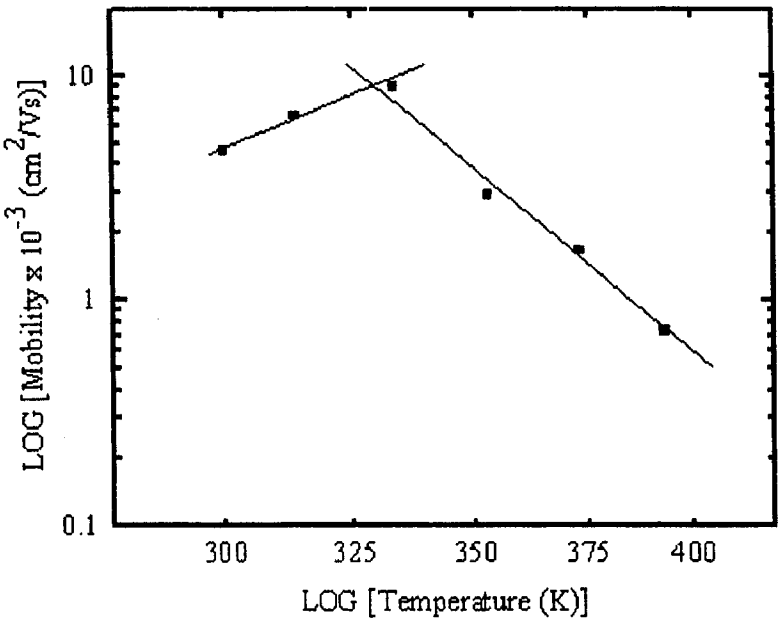


Figure 5-14 Logarithmic relations of mobility and temperature for Fig. 5-13

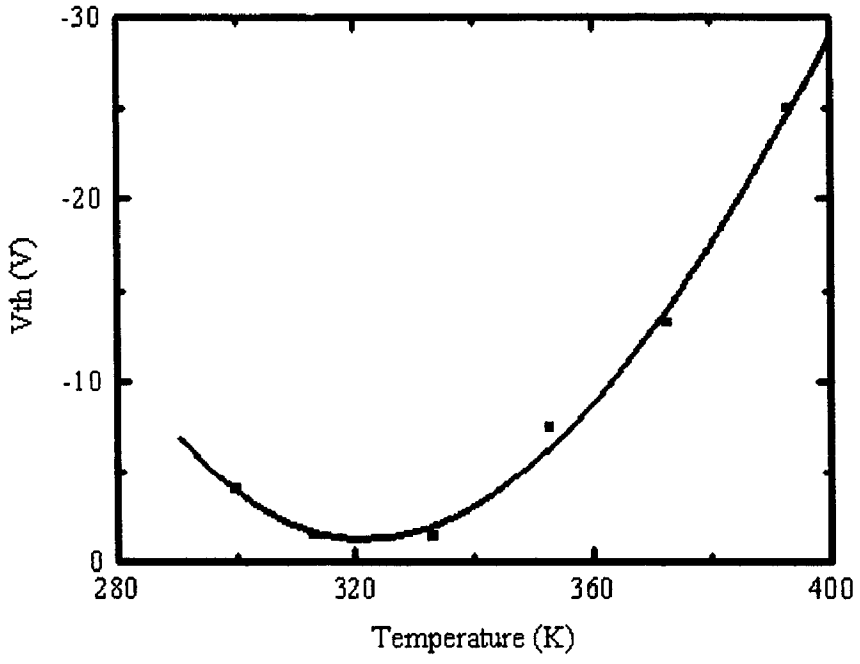


Figure 5-15 Temperature dependence of threshold voltage for pentacene FET

5.3 Pentacene OFETs with SA-SiO_2 as Gate Dielectric

5.3.1 Introduction

In order to have potential applications, OFETs must provide a substantial performance advantage compared with the conventional technology. Among the various OFETs based on organic semiconductors, pentacene OFETs were demonstrated to have the highest mobility and sufficiently high on/off current ratios up to now [20][23]. Moreover, the low-cost and batch fabrication process is extremely necessary in order to benefit the various advantages of the OFETs. Furthermore, the low-temperature process is required due to the thermal properties of the organic materials. And SiO_2 is the most widely used gate dielectric. However, the depositions of SiO_2 in the previous works were done either by the high temperature thermal oxidation, or through LPCVD, PECVD, or through e-beam sputtering which requires a complex system.

In recent years, self-assembly technology has gathered a lot of attention in the fabrication of nanometer scale electronic devices because it is a very easy and low-temperature process that almost eliminates any expensive and complex facilities [79][80][81]. In this work, a simple, low-temperature and low-cost fabrication procedure of pentacene OFETs is presented. The vertical dimension of the self-assembled thin film can be precisely controlled. Unlike the conventional process, the layer-by-layer (LBL) self-assembly allows one to obtain the thin films for a semiconductor device with a dramatically lower temperature, lower cost, and shorter processing time.

5.3.2 Experimental

The high quality insulator with a low leakage current through it and a high breakdown voltage is an important requirement for good performance of a FET. Fig. 5-16

shows the electrical characteristic of Au/self-assembled SiO_2/n^+ heavily doped Si structure shown as the inset of Figure 5-16. Positive bias is defined here as negative voltage applied to the silicon substrate. The 10 layers of SiO_2 nanoparticles were self-assembled and a gold electrode, 80 nm thick, was sputtered. Since the breakdown field was larger than 0.57 MV/cm and the leakage current was typically 2 nA/mm^2 with an applied voltage of 20 V from the analysis of electrical characteristics shown in Figure 5-16, it indicates that self-assembled SiO_2 can be used as a gate dielectric instead of thermal oxidized or sputtered silicon dioxide.

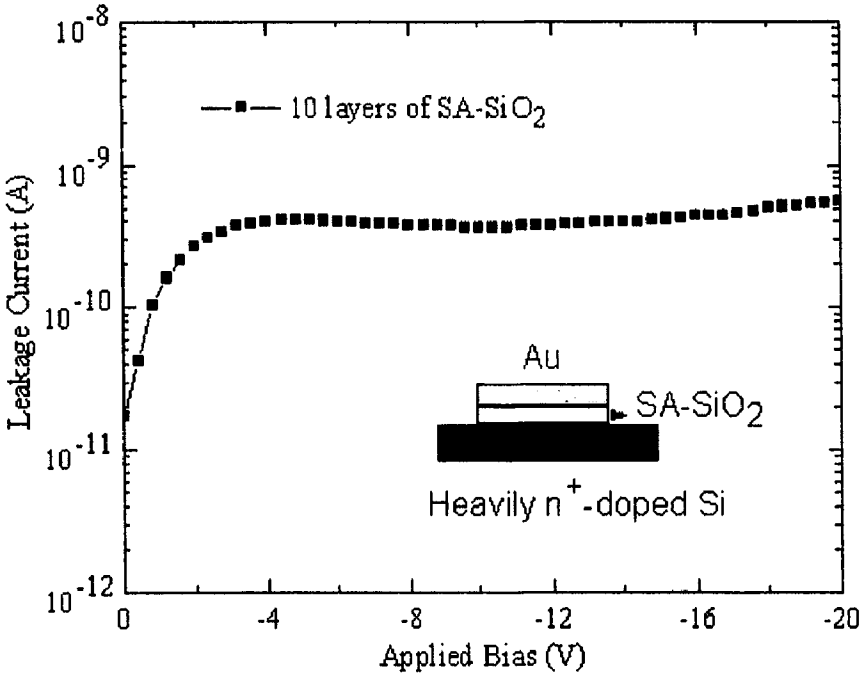


Figure 5-16 Gate leakage characteristic of Au/(SA-SiO_2)/Heavily-doped Si structure

To build pentacene OFETs with self-assembled SiO_2 (SA-SiO_2) as the gate dielectric shown in Figure 5-17, an n^+ heavily doped silicon wafer (resistivity of about 0.001 Ω·cm) was used as a gate electrode and the substrate. After the cleaning of the

silicon wafer surface and H_2SO_4-H_2O_2 treatment for 1 hour, the dielectric layer was self-assembled with SiO_2 nanoparticles that were 45 nm in diameter.

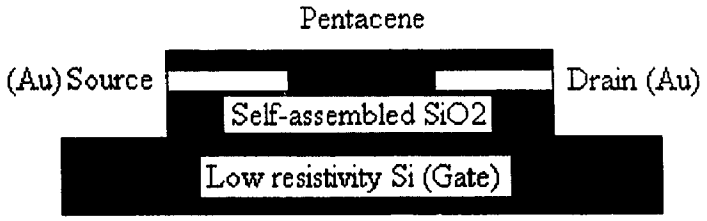
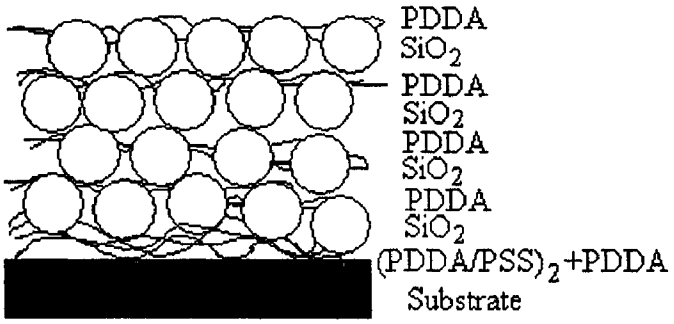
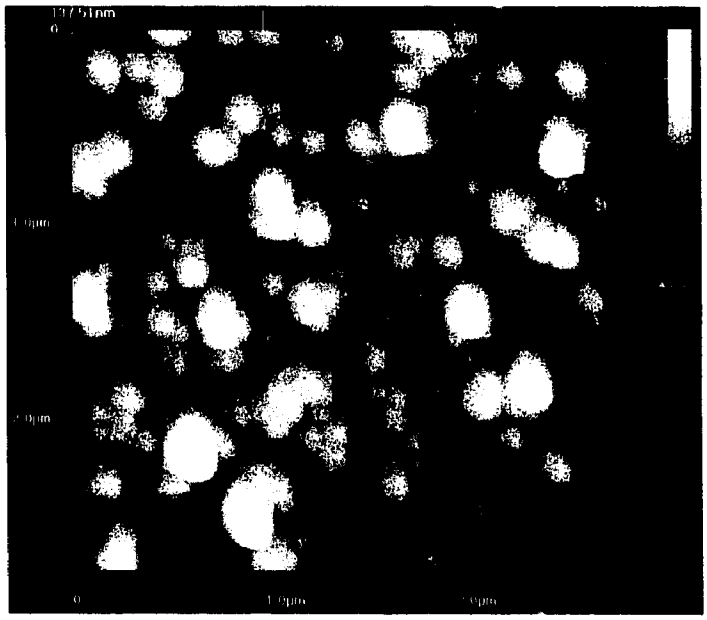


Figure 5-17 Schematic structure of Pentacene FET with SA-SiO_2 as gate dielectric

The silicon substrate was immersed into a 50 ml poly(dimethyldiallylammonium chloride) (PDDA) solution for 20 minutes. Following that, it was rinsed in de-ionized (DI) water for 1 minute, and dried by a nitrogen flow. It was then immersed in a 50 ml polystyrene (PSS) solution for 10 minutes, rinsed and dried as in the previous step. Then the immersion into PDDA was repeated for 10 minutes. The sequence was done as {PDDA (20 minutes) + [PSS (10 minutes) + PDDA (10 minutes)]$_2$}, i.e. dipping in PSS and PDDA were carried again after the first three steps. The intermediate rinsing and drying are necessary. Thus up to date the outermost layer was a positively charged PDDA. After the precursor mutilayer, the substrate was immersed in 50 ml diluted SiO_2 (45 nm in diameter) colloidal dispersions (231 mg/ml, Nissan Kagaku, Japan) with a concentration of 5 mg/ml for 5 minutes, rinsed and dried, followed by another cycle of PDDA (10 minutes). Therefore, the complete sequence of adsorption is {PDDA (20 minutes) + [PSS (10 minutes) + PDDA (10 minutes)]$_2$} + [SiO_2 (5 minutes) + PDDA (10 minutes)]$_{10}$. Figure 5-18(a) shows the schematic diagram of the device with four layers of self-assembled SiO_2 nanoparticles, and Figure 5-18(b) illustrates the self-assembled SiO_2 thin film.



(a)



(b)

Figure 5-18 (a) Schematic SiO_2 self-assembly process, (b) AFM image of SA-SiO_2

Upon finishing the self-assembly of SiO_2 layer as the gate dielectric, a layer of Au, 80 nm thick, was sputtered onto the top of gate dielectric and then patterned to form the source and drain electrodes as shown in Figure 5-17. Finally, the Pentacene-based OFETs were completed with the deposition of a layer of about 200 nm thick pentacene as an organic semiconductor. Pentacene was thermally evaporated through a shadow mask with a low deposition rate and a working pressure of 6×10^{-7} Torr. The pentacene material

is commercially available from Aldrich Chemical (98%) and used without performing any further purification process. During the evaporation of pentacene, the substrate was held at room temperature. With the purification of the pentacene material and moderation of the substrate heating as described in previous works, the electrical characteristics of the fabricated FETs could be much improved as expected [5].

5.3.3 Result and Discussion

A quartz crystal microbalance (QCM) equipment produced by USI System in Japan was used to monitor the LBL assembly process of silica nanoparticles. It is a microbalance suitable to detect the tiny mass and thickness adsorbed on its face. It senses the resonance frequency directly, which results in a high sensitivity. The following relationship is obtained between adsorbed mass M (g) and frequency shift ΔF (Hz) by taking into account the characteristics of quartz resonators used:

$$\Delta F = -1.83 \times 10^8 M/A \qquad (5\text{-}1)$$

where A is the apparent area of quartz microbalance placed between QCM electrodes. This is 0.16 ± 0.01 cm^2 in our system. The thickness of the alternate layer corresponding to QCM frequency shift was determined by SEM observation of the film's cross-section from SEM images of cut resonators coated with silicon/polycation films, which gives the following relationship with ±5 % error [82]:

$$d\ (nm) = 0.022\ (-\Delta F)\ (Hz) \qquad (5\text{-}2)$$

The accumulative frequency shift for 10 layer silica nanoparticles is obtained to be 16023 Hz. Based on equation (5-2), the total thickness of the dielectric layer was calculated as 353 nm.

It was found that the dielectric constant was slightly higher than the one for thermal oxide. The SiO_2/PDDA film volume composition is: 70 % SiO_2 + 10 % polycation + 20 % air-filled pores. These pores are formed by closely packed 45-nm SiO_2 and have a typical dimension of 15 nm [81]. Therefore, the dielectric constant of the multilayer was higher due to about 30% of inclusions, such as air, polyion layers, etc. If the layer of silicon dioxide were produced by conventional thermal oxidation, the dielectric constant would be 3.9. Otherwise, the dielectric constant of the multiplayer formed by LBL nano-assembly is around 6 [81].

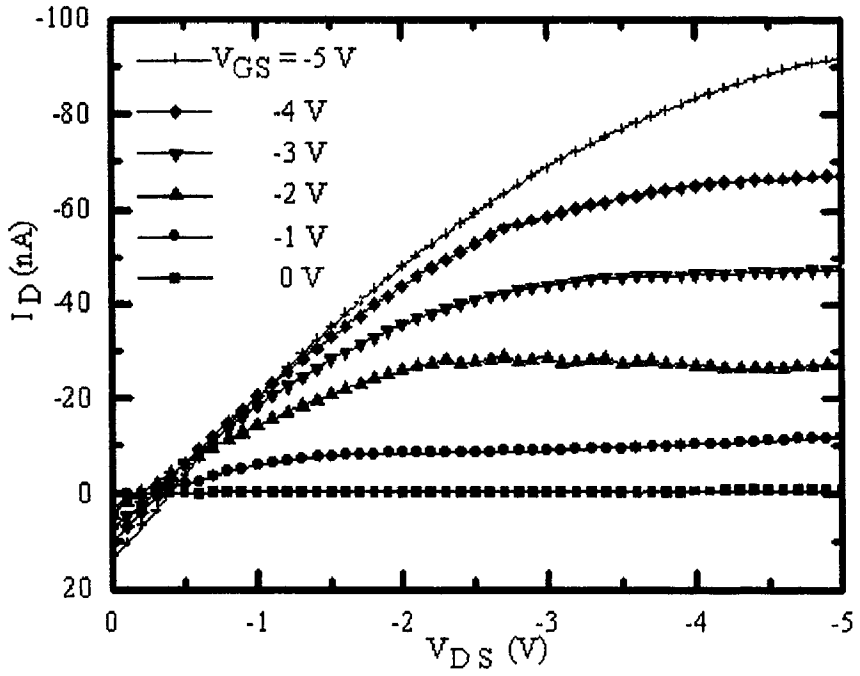


Figure 5-19 Drain characteristics of pentacene FET with SA-SiO_2 as insulator

I_D-V_{DS} drain characteristics of a typical pentacene FET fabricated with SA-SiO_2 as the gate dielectric are shown in Figure 5-19. This device has a channel length and width of 25 and 500 μm, respectively, and a gate dielectric layer 353 nm thick. In pentacene OFETs, the current between drain and source I_D is controlled by the applied

gate-source voltage V_{GS}. Since pentacene is a p-type polymeric semiconductor, pentacene FETs generally operate in the accumulation mode with the negative bias on drain-source and gate-source electrodes. The negative gate bias will enlarge the conduction channel due to the formation of a hole accumulation layer. Thus, the conductivity of the channel between drain and source is increased with the negative gate bias.

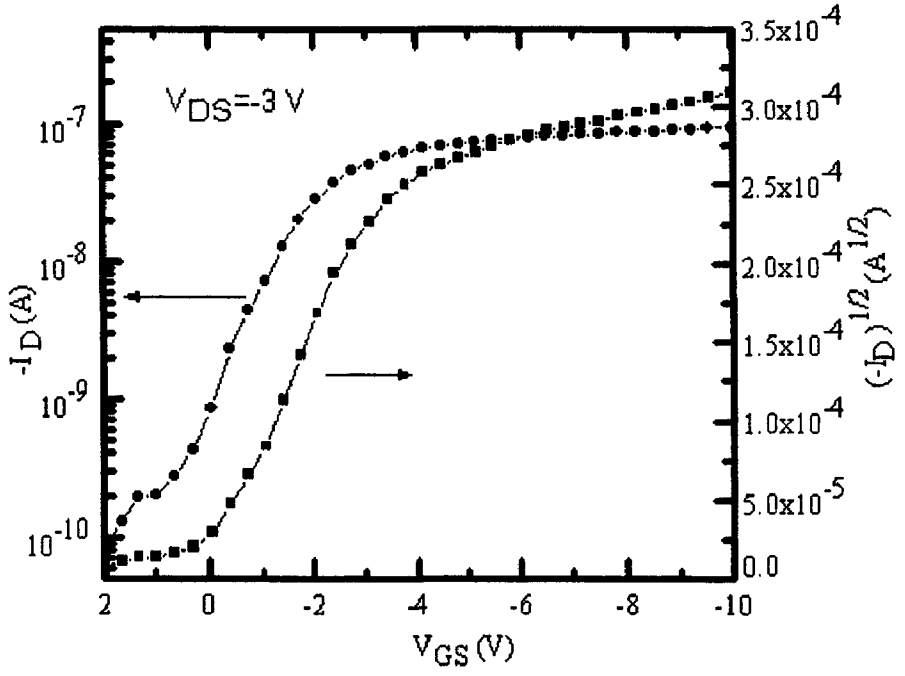


Figure 5-20 Gate characteristics of pentacene FET with SA-SiO_2 as insulator

Fig. 5-20 shows the measured gate transfer characteristics of the same pentacene OFET described above. The field-effect mobility is generally determined in the region where the drain current saturates according to the equation (4-2). From the slope of the square root of the saturation current as a function of the gate voltage as shown in Figure 5-20, a field-effect mobility of 0.05 cm^2/Vs was extracted at the small V_{DS} of -3 V. By linearly extrapolating the curve to the V_{GS} axis, the threshold voltage V_{th} can be found to be 0.3 V. When the V_{DS} of -3 V was applied and the gate voltage were swept from 2 V to

-10 V, the threshold slope was obtained to be about 1.4 V/decade and the on/off current ratio was about 10^3.

In brief, a low-cost and low-temperature fabrication process of pentacene OFETs has been presented using self-assembled SiO_2 as a gate dielectric material. Self-assembly may pave the way to replace the thermal oxide as gate dielectric that eliminates the expensive facilities such as the oxidation furnace or sputtering system.

5.4 Performance Improvement of Pentacene OFETs

5.4.1 Introduction

In general, the performance of OFET was determined by the properties of active semiconductor film, especially the region near the dielectric-semiconductor interface. For the polycrystalline pentacene film, the previous research revealed the charge transport would strongly depend on the molecular ordering within the film, the trapped charge at grain boundaries [83], and the morphology of the semiconductor layer [84]. To improve the OFET performance, it is necessary to reduce the density of trapping sites and gas-adsorption sites, and to promote molecular ordering for better film properties. In some previous works, researchers improved the electrical characteristics of OFETs through the purification of the pentacene material, octadecyltrichlorosilane (OTS) treatment of dielectric surface, and moderation of the substrate heating [5]. Here, the effect of oxygen plasma treatment of dielectric layer was investigated with a purpose of improving performance of OFET by a simple method.

5.4.2 Experimental

An n^+- doped silicon wafer as a gate was thermally oxidized to form a layer of SiO_2 of 100 nm thick. And then a layer of Au was sputtered on the SiO_2 and then

patterned to form the source and drain electrodes. Then it was put into the mild oxygen plasma (150 W) for 5 minutes. Finally, pentacene, 150 nm thick, was thermally evaporated through a shadow mask under the pressure of 6×10^{-7} Torr. As a comparison, a pentacene FET was fabricated in the same procedure but without O_2 treatment.

5.4.3 Result and Discussion

Figure 5-21 and Figure 5-22 show the electrical characteristics of a pentacene FET without oxygen plasma treatment on the dielectric surface. With oxygen plasma treatment, pentacene FET has the electrical characteristics as shown in Figure 5-23 and Figure 5-24. The dimensions of the FETs were the same with a channel length of 75 μm and a width of 1000 μm. The main parameters were extracted as shown in Table 5-2.

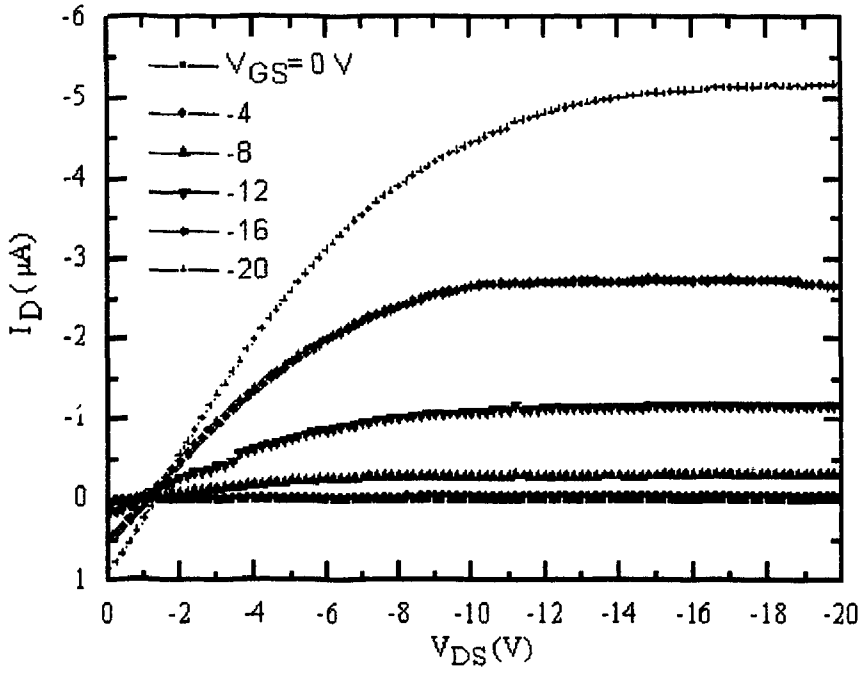


Figure 5-21 Drain characteristics of pentacene FET without O_2 plasma treatment

With oxygen plasma treatment, the field-effect mobility could be increased as well as a lower down threshold voltage and higher drain current. This performance

promotion might come from a cleaner and smoother dielectric surface that will benefit the deposition of pentacene for a higher molecular ordering film. From the experiments, a summary can be reached that oxygen plasma treating of an oxide surface could improve the FET performance with higher mobility, lower V_{th}, and larger drain current.

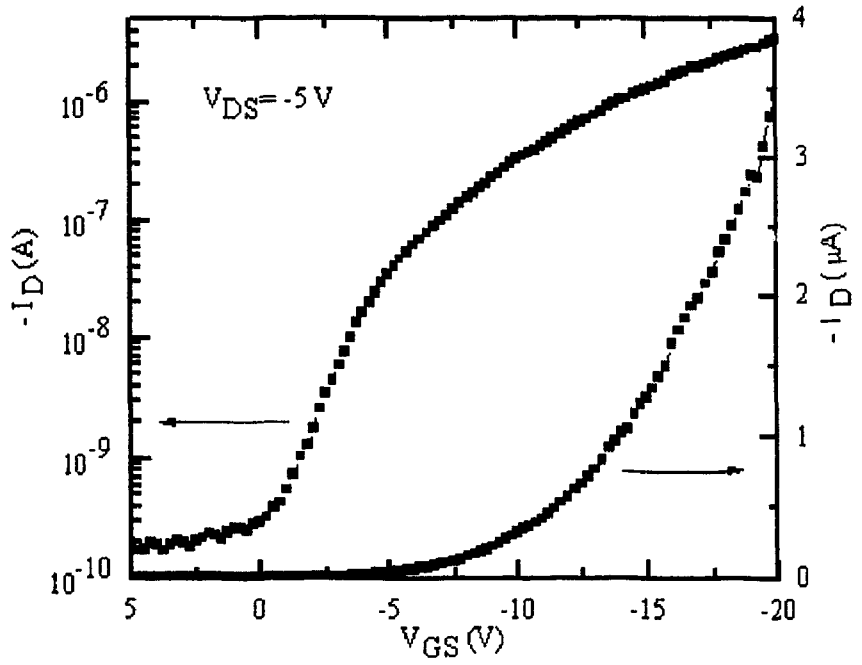


Figure 5-22 Gate characteristics of pentacene FET without O_2 plasma treatment

Further research for increasing field-effect mobility of pentacene OFETs, some methods could be investigated to obtain the improved molecular ordering, grain size, or morphology of the semiconductor, or reduced surface roughness of gate dielectric. For example, the dielectric surface may be treated with self-assembled monolayer for a well defined, ordered surface prior to the pentacene deposition. And another way is to use a very thin layer of dielectric in nanometer scale with a smooth surface or molecular alignment by the artificial surface pattern as a buffer layer of gate dielectric. Pre-patterning of buffer layer in nanometer scale ordering might result in the defect

segregation to the boundaries of pre-patterned grains, which might reduce the defects and trap density in the deposited semiconductor.

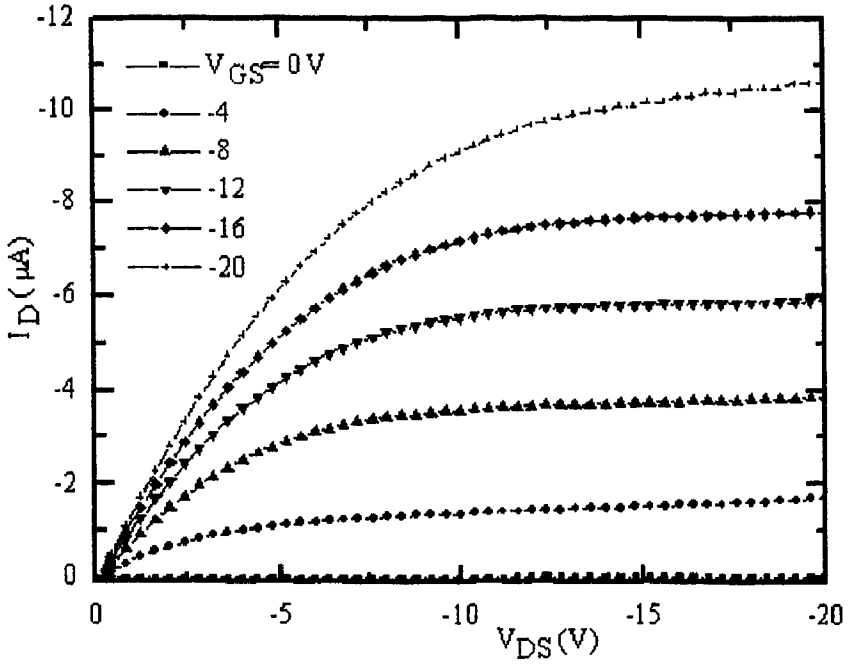


Figure 5-23 Drain characteristics of pentacene FET with oxygen plasma treatment

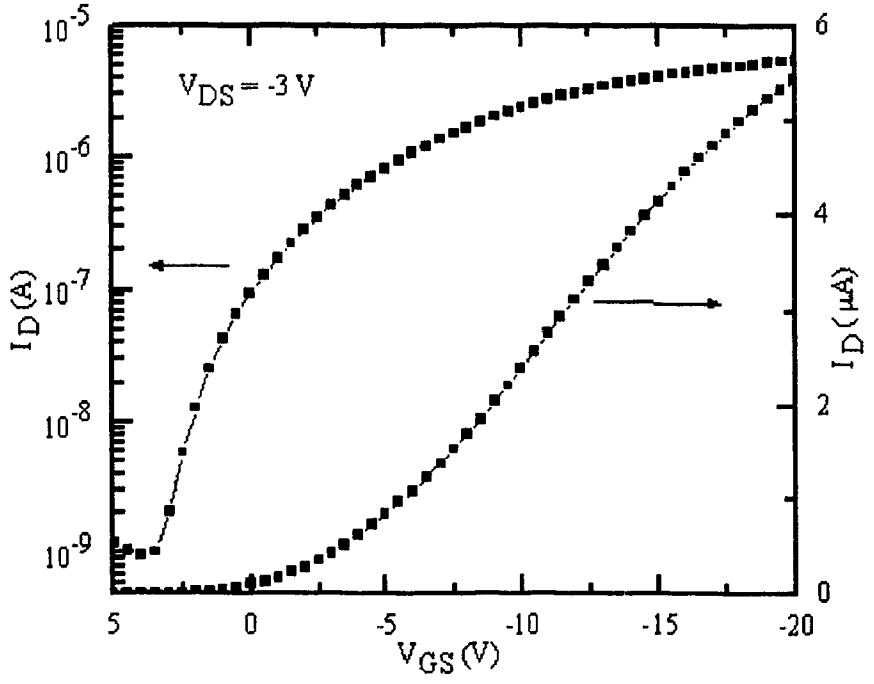


Figure 5-24 Gate characteristics of pentacene FET with oxygen plasma treatment

Table 5-2 Main parameters of pentacene FETs

	μ_{FET} (cm^2/vs)	V_{th} (V)	Slope (V/Dec)	Ion/Ioff
With O_2 plasma	0.16	-2	2	1.67×10^4
Without O_2 plasma	0.11	-6	2	2.01×10^4

5.5 Dual-Gate Pentacene OFETs

5.5.1 Introduction

In this section, a simple, low-temperature and low-cost fabrication procedure of Dual-gate OFETs is presented. A dual-gate pentacene FET with 8 layers of SiO_2 nanoparticle and thermal oxide, 100 nm thick, as the gate dielectric was presented as shown in Figure 5-25 with good performance. Self-assembly technology was used to deposit the top gate dielectric layer formed with SiO_2 nanoparticles.

5.5.2 Experimental

To build dual-gate pentacene OFETs with SA-SiO_2 as the gate dielectric shown in Figure 5-25, a heavily doped silicon wafer was used as a bottom-gate electrode and the substrate. The silicon wafer was thermally oxidized to form a layer of SiO_2 of 100 nm thick. Then a layer of Au, 80 nm thick, was sputtered onto the top of SiO_2 and then patterned to form the source and drain electrodes. Pentacene, about 200 nm thick, was thermally evaporated without any purification through a shadow mask with the low deposition rate and working pressure of 6×10^{-7} Torr. During the evaporation of pentacene, the substrate was held at room temperature. Upon this point, the bottom part of the dual-gate pentacene FET was formed. Then, the dielectric layer was self-assembled with SiO_2 nanoparticle with the size of 45 nm. The assembling process of dielectric layer

was described in detail in section 5.3. The thickness of the final SiO_2 layer is about 300 nm. Upon finishing the self-assembly of SiO_2 layer as the top-gate dielectric, a layer of Al, 150 nm thick, was evaporated onto the top of the gate dielectric and then patterned to form the top-gate electrode as shown in the Figure 5-25.

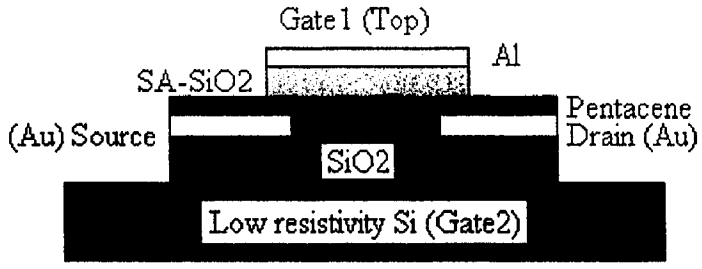


Figure 5-25 Schematic cross-section view of dual-gate pentacene OFETs

5.5.3 Result and Discussion

Figure 5-26 and figure 5-27 show the drain characteristics and the gate characteristics of a dual-gate pentacene FET, respectively. This FET has a channel length of 25 μm and a channel width of 800 μm. By analyzing experimental data with the method described in Chapter 4, the main parameters of this device were extracted to be: V_{th} of -2.2 V, μ_{FET} of 0.1 cm^2/Vs, slope of 1.3 V/decade, and I_{on}/I_{off} of 3.8×10^3.

For the same dual-gate pentacene FET, the characteristics of its bottom part that is also a FET structure were also measured and investigated. Its drain and gate characteristics were shown as Figure 5-28 and Figure 5-29, respectively. From these figures, this FET has a field-effect mobility of 0.02 cm^2/Vs at V_{DS} of –3 V, a threshold voltage of -2 V, a slope of 2 V/decade, and an I_{on}/I_{off} of 3.2×10^3.

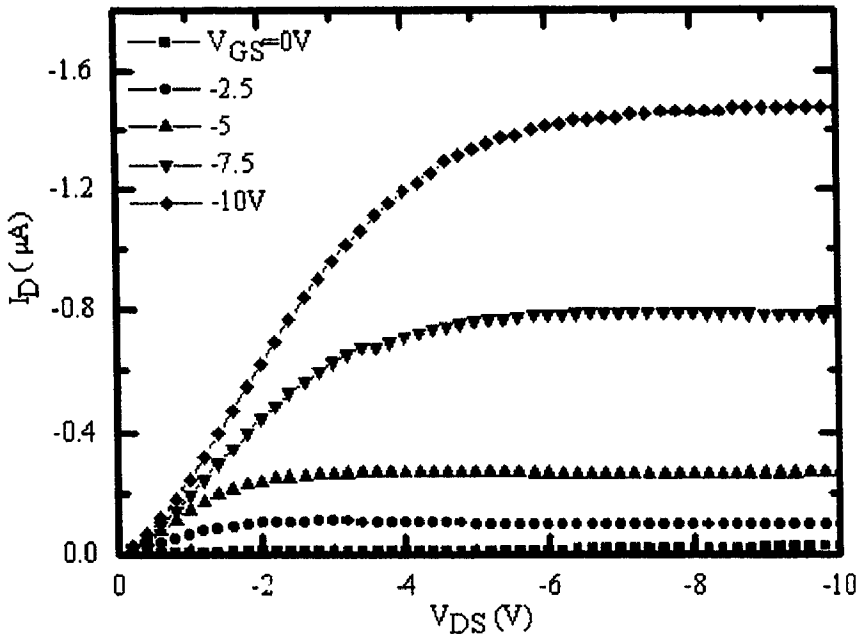


Figure 5-26 Drain characteristics of dual-gate pentacene FET

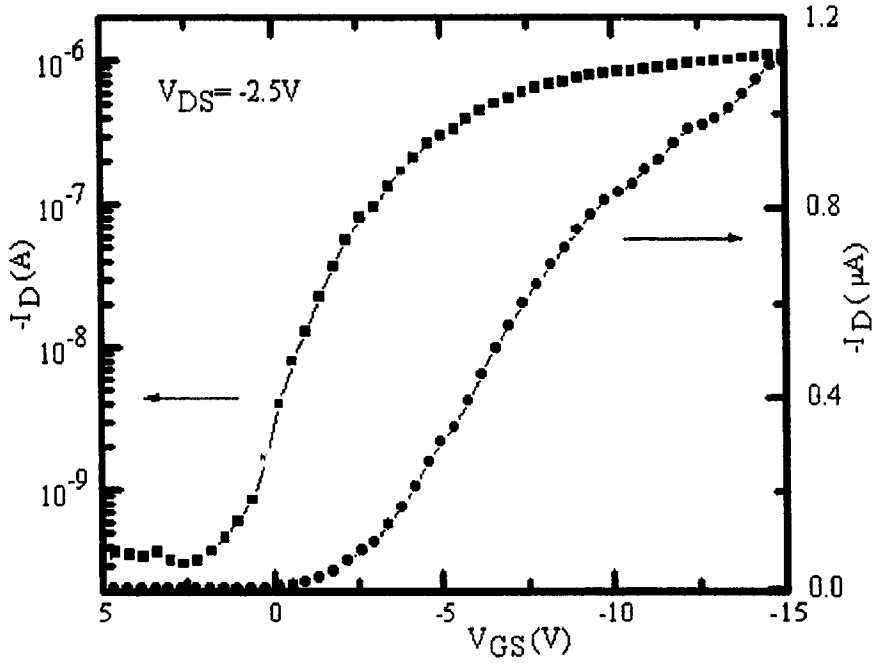


Figure 5-27 Gate characteristics of dual-gate Pentacene FET

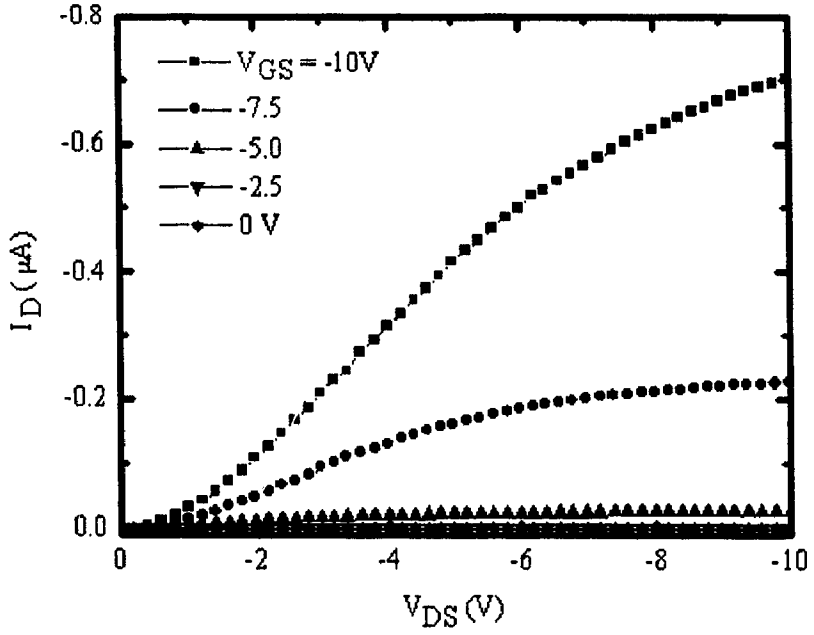


Figure 5-28 Drain characteristics of bottom part of dual-gate pentacene FET

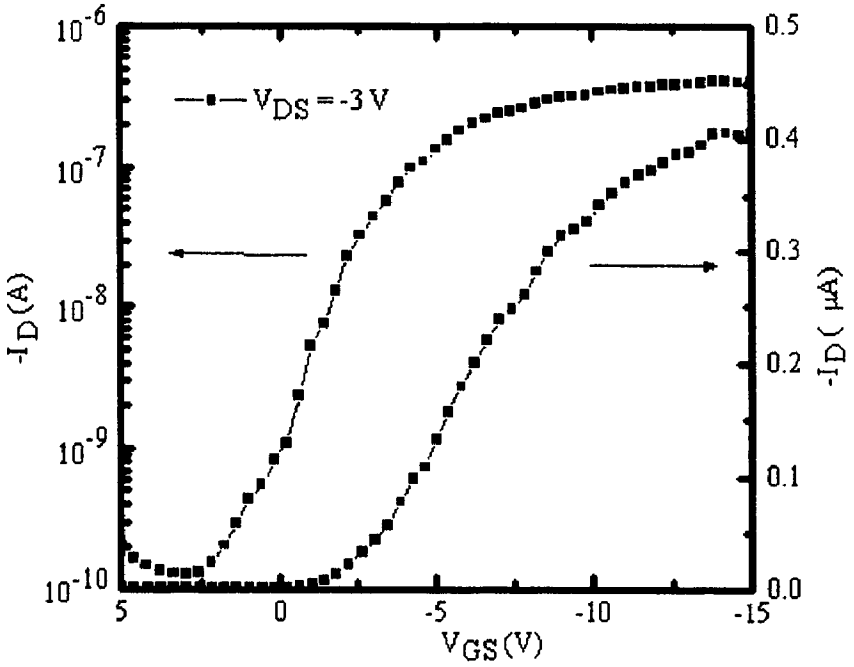


Figure 5-29 Gate characteristics of bottom part of dual-gate pentacene FET

From this experiment, it can be found that the dual-gate FET demonstrates a better performance compared with a single gate FET. It shows that the dual-gate FET performs well with high drain output current at relative low operating voltage, large field-effect mobility, and channel controllability by separately adjusting two gate biases. The dual-gate can be considered to be composed of a top FET and a bottom FET, with two conduction channels (assuming thick semiconductor film), and may display about twice the drain output current of a single gate FET.

This kind of dual-gate FET may be useful in organic optoelectronics and displays as a driving device, or a memory device, and so on. The main advantages of dual-gate FET are: (1) higher drain current for the output; (2) large field-effect mobility which means a faster switching speed; (3) better gate-transfer control.

5.6 Pentacene OFET Based Inverter Circuit

5.6.1 Introduction

There are some reports on the fabrication of OFET based electronic circuits such as inverter, ring oscillator, code generator and decoder, shift register, transmission gate [7][11][20][21][85]. Based on the studies of pentacene OFETs, here a simple inverter circuit has been fabricated consisting of pentacene FET and ink-jet printed polymer resistor.

Ink-jet printing (IJP) has emerged as an attractive patterning technique with advantages over other techniques with respect to low-cost, adaptable, non-contact and large area direct printing without mask. IJP has already been used for fabricating polymer light-emitting devices [28][86], organic FETs and circuits [87].

5.6.2 Experimental

In this work, n+ heavily doped silicon wafer was used as the gate and substrate. Silicon dioxide with 100 nm thicknesses was formed by thermal oxide to function as the gate dielectric. Then a layer of Au, 80 nm thick, was deposited and patterned as the source and drain electrodes. Pentacene semiconductor of around 150 nm was deposited by thermal evaporation under the high vacuum through a shadow mask. The fabricated pentacene FET has a structure as shown in Figure 5-1(b).

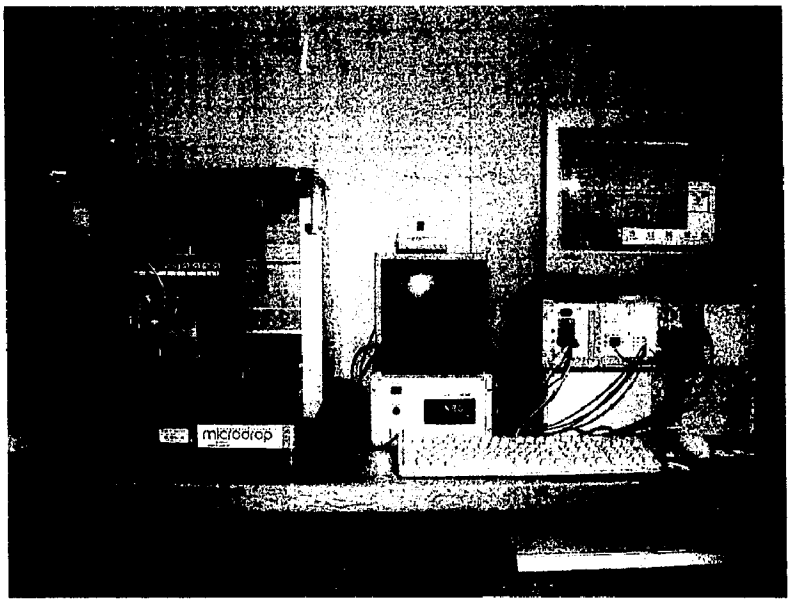


Figure 5-30 Ink-jet printing system by Microdrop for polymer resistor printing

Ink-jet printing technique was used to print the polymer resistor. Here the PPy was used as the conductive polymer since it is good for ink-jet printing. Three layers of PPy were ink-jet printed by our ink-jet printing system from Microdrop, as shown in Figure 5-30, to form the load resistance, Rd, shown in Figure 5-31 and Figure 5-33. The resistance value can be adjusted over a wide range by varying the concentration of PPy and the number of layers. Figure 5-31 shows the optical images of constructed inverter

circuit without resistor (Left) and with resistor and bonded wire (Right). A circuit array and an IC package are shown as Figure 5-32.

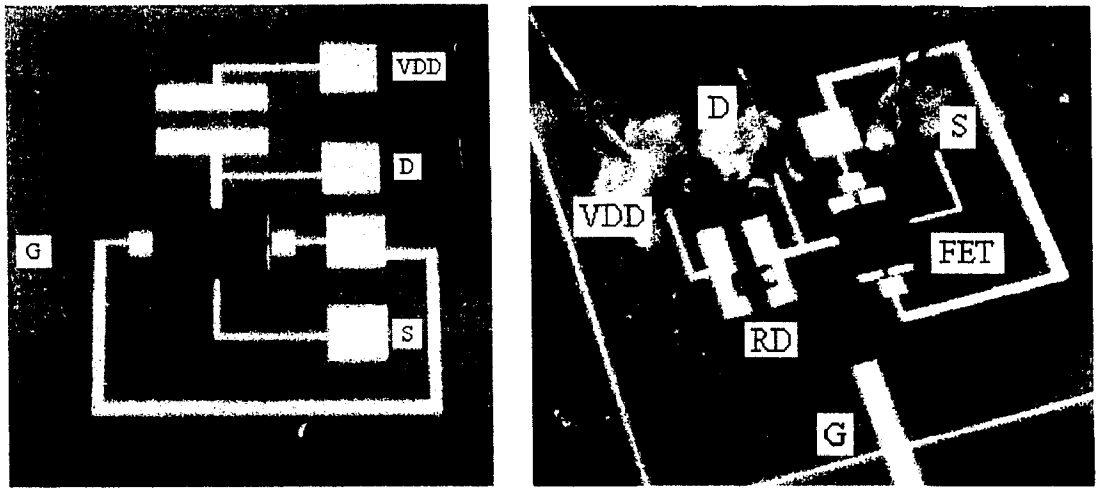


Figure 5-31 Optical image of circuit without resistor (Left) and with resistor (Right)

Figure 5-32 Optical image of fabricated circuit array (Left) and IC package (Right)

5.6.3 Result and Discussion

Figure 5-33 shows the polymer inverter circuit schematic diagram. The voltage transfer characteristics of an integrated pentacene inverter are shown in Figure 5-34. The logic states of polymer inverter were summarized in Table 5-3. It shows the clear inverter

action for switching between logic "1" and logic "0". This inverter has a small gain of about 1. Higher gains could be obtained by increasing the load resistance, Rd.

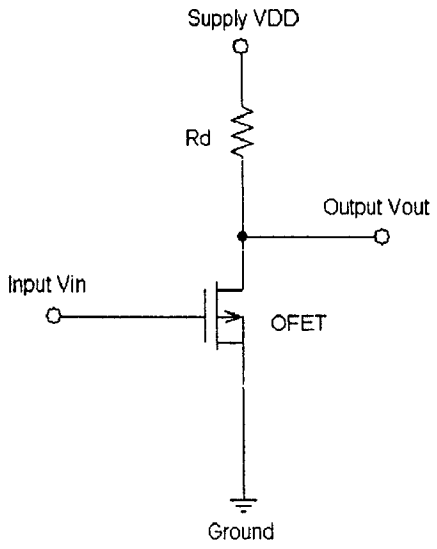


Figure 5-33 Circuit diagram of pentacene inverter

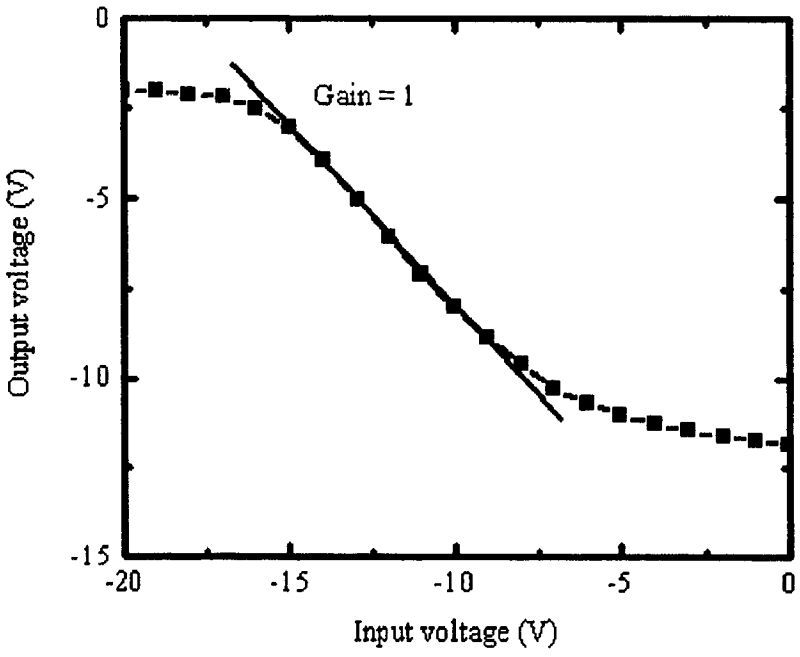


Figure 5-34 Transfer characteristics of pentacene inverter

For practical application, further improvement is needed. In particular, since the whole silicon wafer is used as the gate, capacitance can exist between the gate and the source/drain electrodes as well as between the gate and connection wires and Rd. These may affect the accumulation layer and carrier injection. In addition, some methods described in previous sections are needed to achieve higher field-effect mobility and low threshold voltage for improved circuits. The polymer resistor may be replaced with an OFET as the load to promote the circuit performance. With further improvement, it could be applied in applications such as active-matrix displays or identification tags.

Table 5-3 Logic table for inverter

Vin (V)	Vin logic state	Vout (V)	Vout logic state
-20	1	-2	0
0	0	-12	1

In a word, a simple electronic circuit has been realized by integrating pentacene based FET and ink-jet printed polymer resistor. Simple inverters, with a voltage gain of about one, have been demonstrated as one of various applications of the organic devices.

CHAPTER SIX

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

A variety of organic devices including polymer Schottky diode, all-organic diodes, PEDT/PSS-based transistors, pentacene OFETs, dual-gate OFETs, and organic inverter circuit, using the microfabrication techniques such as traditional photolithography, spin coating, evaporation, reactive ion etching, ink-jet printing, and self-assembly, have been realized.

A simple fabrication procedure consisting of spin-coating and reactive ion etching with metal as the pattern mask has been developed to fabricate organic diodes and PEDT/PSS-based transistors. It eliminates the influence of chemical solvent on the device.

Layer-by-layer self-assembly technique has been used to form the gate dielectric as an alternative insulator of silicon dioxide for the fabrication of pentacene OFETs. From this investigation, the dielectric film of assembled SiO_2 nanoparticles shows the good properties with high breakdown voltage and low leakage current. It may also be suitable for the fabrication of organic devices and circuits with low cost, simple process, and inexpensive facility needs.

Based on pentacene OFETs, the temperature dependence of mobility and threshold voltage have been investigated in the range from 300 K to 400 K. A method to promote a device's mobility has also been studied. Moreover, a dual-gate pentacene FET has been developed as a new device structure with high performance. In the last part, a simple inverter circuit integrated with a pentacene FET and an ink-jet printed polymer resistor has been fabricated to show one of the applications of organic devices.

6.2 Advantages and Future Work

Although organic electronics could not compete with traditional silicon-based electronics, several advantages of the organic device are observed in experiments as follows:

(1) Low cost and simple process;

(2) Large area coverage;

(3) Light weight and mechanical flexibility;

(4) Rapid and high volume batch fabrication.

For organic devices to be commercialized to practical applications, some future research works are worthy to be addressed.

Firstly, while many experimental investigations of carrier transport in organic devices have been reported and several models have been developed, the theoretical understanding of charge transport in organic thin films is still complicated and difficult. Consequently, it is still impossible to predict precise macroscopic properties such as current-voltage characteristics from the given energy levels and charge transport mobilities of the materials. There is also no complete quantitative description for the field and temperature dependence of charge mobility in amorphous organic materials.

Techniques to produce organic crystalline thin films should be developed to significantly forward the technology of organic electronics. Increased molecular order improves carrier transport, lowering operating voltage and increasing the charge injection efficiency.

Secondly, the interfaces of Organic/Organic, Organic/Metal, and Organic/Dielectrics and doping effect are necessary to be investigated for improvement of a device's performance since they are important factors that affect the device's characteristics.

Thirdly, stability of a device should be much improved to prolong the device's lifetime. It could be solved by synthesizing new organic semiconductors with high stability and mobility, especially air-stable n-type semiconductors for the complement circuits.

Furthermore, new device structures and new fabrication techniques need to be generated for devices with smaller feature size. To successfully compete with amorphous and low temperature polysilicon devices, organic electronics must be made as small as possible using simple and low-cost fabrication techniques. Conventional technologies can define horizontal feature size less than quarter micron. However, the process becomes more expensive when the device's area increases. In contrast, it is relatively easy to control the thin film thickness over a large area. Therefore, vertical device structures may be considered as a new direction of further research. For example, a vertical polymer FET by embossing has been reported [88]. Here, self-assembly technique might be a promising method to form an extremely thin film over the large area and even on the sidewall of a gate dielectric layer of the vertical OFETs. Other microfabrication

techniques are worthy to be developed to define critical features with submicrometer resolution. To continue the growth of organic-based electronics, it is important to find new applications, such as organic photovoltaics, photodetectors, organic lasers, organic memory device, chemical sensors, and organic biosensors.

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