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FABRICATION, CHARACTERIZATION, AND MODELING OF ORGANIC CAPACITORS, SCHOTTKY DIODES, AND FIELD EFFECT TRANSISTORS

By

Mo Zhu, B. S.

A Dissertation Presented in Partial Fulfillment of the
Requirement for the Degree of
Doctor of Philosophy in Engineering

COLLEGE OF ENGINEERING AND SCIENCE
LOUISIANA TECH UNIVERSITY

August 2004

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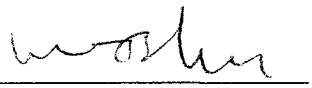
Author 

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ABSTRACT

The objectives of this project are to fabricate, characterize, and model organic microelectronic devices by traditional lithography techniques and Technology Computer Aided Design (TCAD).

Organic microelectronics is becoming a promising field due to its number of advantages in low-cost fabrication for large area substrates. There have been growing studies in organic electronics and optoelectronics. In this project, several organic microelectronic devices are studied with the aid of experimentation and numerical modeling.

Organic metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) capacitors consisting of insulating polymer poly(4-vinylphenol) (PVP) have been fabricated by spin-coating, photo lithography, and reactive ion etching techniques. Based on the fabricated devices, the dielectric constant of the (PVP) is calculated to be about 5.6 – 5.94. The MIS capacitor consisting of organic semiconductor pentacene has been investigated. The hole concentration of pentacene is determined to be around 8×10^{16} cm^{-3}.

Schottky diodes consisting of aluminum and a layer of p-type semiconducting polymer poly[2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene] (MEH-PPV) have been fabricated. Based on the current-voltage (I-V) and capacitance-voltage (C-V) measurements, the temperature dependence of hole mobility in MEH-PPV has been extracted by the space-charge limited conduction (SCLC) model, from 300 to 400 K.

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Moreover, the value of the effective hole density for MEH-PPV has been determined to be 2.24×10^{17} cm^{-3}. Numerical simulations have been carried out to identify the parameters which affect the performance of devices significantly.

Organic n- and p-channel field-effect transistors (FETs) have been designed and fabricated. By using Naphthalene-tetracarboxylic-dianhydride (NTCDA) as an organic semiconductor, n-channel FETs have been fabricated and characterized. At room temperature, the device characteristics have displayed electron mobility of 0.016 cm^2/Vs, threshold voltage of -32 V, and on/off ratio of 2.25×10^2. Pentacene, an organic semiconductor offering high device performance, has been employed to fabricate the p-channel FETs. At room temperature, the device characteristics have displayed hole mobility of 0.26 cm^2/Vs, threshold voltage of -3.5 V, subthreshold slope of 2.5 V/decade, and on/off ratio of 10^5. The temperature and field dependence of mobility has been studied based on the experimental results. Based on numerical simulations, the influence of bulk traps has also been identified, and the field-dependent mobility model has been used to obtain more accurate simulation results. Furthermore, electrostatically assembled monolayer (poly(dimethyldiallylammonium chloride) (PDDA)) is introduced at the organic/insulator interface to improve the performance of the FETs.

The efforts carried out in this work appear to be the first reported attempt at the investigation of the temperature dependence of mobility for the given organic devices, and the surface modification of organic FETs by electrostatically assembled monolayer.

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ACKNOWLEDGEMENTS

I would like to express my lasting gratitude and appreciation to my advisor, Dr. Kody Varahramyan, and my former co-advisor, Dr. Tianhong Cui, who have guided and instructed me in the scientific method and honest attitude. Their invaluable advice, continuous guidance, encouragement, and assistance have been necessary for the completion of this dissertation. Special acknowledgements are extended to Dr. Yi Su, Dr. Debasish Kuila, Dr. Cheng Luo, and Dr. Alfred Gunasekaran, for their advice and serving as advisory committee members of this dissertation.

The author would like to thank the staff at Institute for Micromanufacturing for their help and support with the experimental and simulation parts of this work. Much gratitude is extended to Mr. Abdul Khaliq, Mr. Dee Tatum, Dr. Guirong Liang, and Ms. Jingshi Shi for their valuable discussion, support, and contributions.

My deepest appreciation goes to my parents and my wife. I could not have been what I am today without them. Their love and encouragement accompanied me through this research.

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CHAPTER ONE

INTRODUCTION

1.1 Organic Microelectronics

Organic microelectronics is becoming a promising field due to its number of advantages in low-cost fabrications for large-area substrates. There have been growing studies in organic microelectronics to improve semiconducting, conducting, and light-emitting properties of organics (polymers, oligomers) and hybrids (organic–inorganic composites) through novel synthesis and process techniques. Performance improvements, coupled with the ability to process these active materials at relatively low temperatures over large areas on glass or paper by the ink-jet printing technique, will provide unique technologies, generate new applications, and form factors to address the growing needs for pervasive computing and enhanced connectivity [1].

Conducting polymers have potential applications at almost all levels of microelectronics [2] as shown in Figure 1-1. Conducting polymers have applications in the areas of lithography, metallization, corrosion-protecting coatings for metals, and electrostatic discharge, protective coatings for packages, and housings of electronic equipment. Moreover, two important areas of applications for conducting polymers in the future are their possible use in interconnection technology and as novel organic materials in microelectronic devices.

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Based on the electrical properties of organic materials, they are used to re-fabricate the traditional microelectronic devices, such as capacitors, diodes, transistors and so on, to take the place of traditional inorganic materials in some certain areas. Among these applications, thin film transistors (TFTs) and light-emitting diodes (LEDs) are widely studied. All the abbreviations in this dissertation are listed in Table 1-1 at the end of this chapter. Figure 1-2 and Figure 1-3 schematically show the structures of typical TFTs and LEDs, respectively. Figure 1-4 shows the comparison of mobility between inorganic materials and organic materials. The mobility of organic materials keeps increasing since 1986, achieved by improving the processes or by synthesizing new organic materials [3].

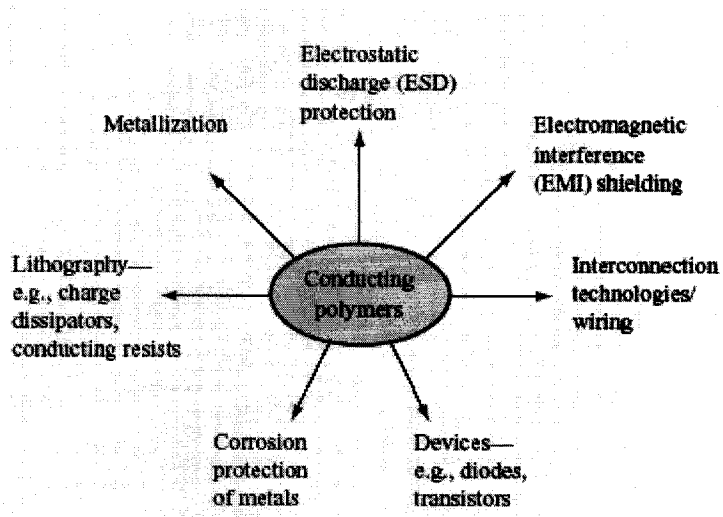

Figure 1-1 Overview of applications of conducting polymers in microelectronics [2].

Efforts on these active materials initiated in academia and in industrial research laboratories in the 1980s have led to a dramatic improvement in performance due to innovative chemistry and processing, as well as the growing ability to understand and control the assembly and ordering of oligomers and polymers. Efforts on semiconducting conjugated organic thiophene oligomers [4][5], thiophene polymers [6][7][8], and the

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small pentacene molecule [9][10][11] have led to improvements in the mobility of these materials by five orders of magnitude over the past three decades as shown in Figure 1-5.

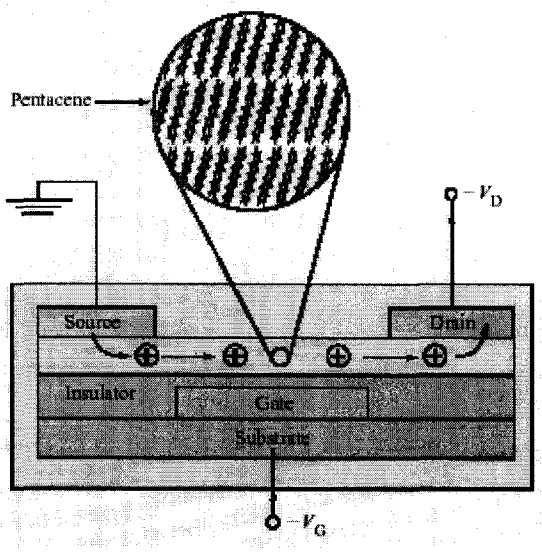

Figure 1-2 Schematic structures of TFTs realized by organic materials [1].

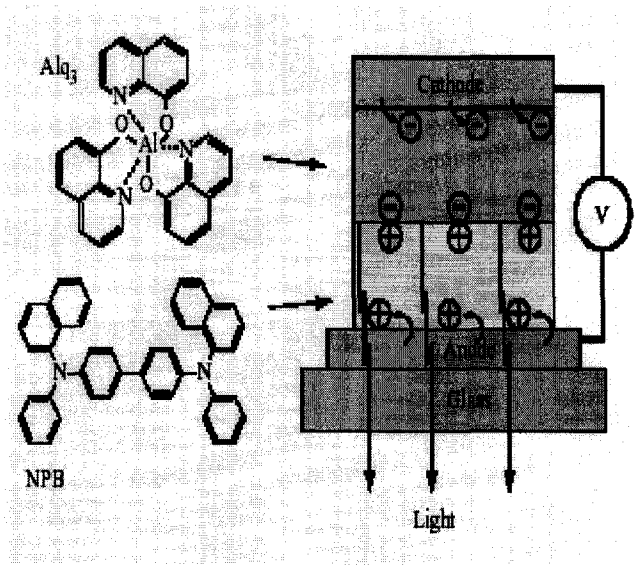

Figure 1-3 Schematic structures LEDs realized by organic materials [1].

Further research is needed to improve the mobility and environmental stability of n-type and p-type materials, as well as the fundamental understanding of electron injection, metal contact, electron transport, surface modification, and self assembly.

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However, organic systems offer a great deal of flexibility in their synthesis, and as chemists develop new materials and learn how to better order and process them, it is hoped that mobility will continue to improve, perhaps reaching the performance of polysilicon and expanding the applications of such materials for low-cost logic chips.

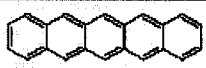
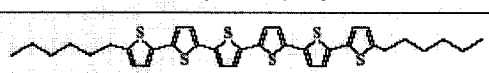
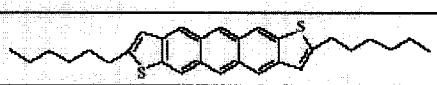
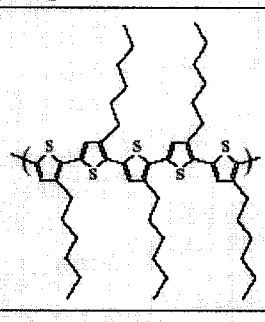
Semiconductor	*Representative chemical structure*	*Mobility* ($cm^2V^{-1}s^{-1}$)
Silicon	Silicon crystal	300–900
	Polysilicon	50–100
	Amorphous silicon	~1
Pentacene		~1
α,ω-dihexyl-sexithiophene		10^{-1}
α,ω-dihexylanthra-dithiophene		10^{-1}
Regioregular poly(3-hexylthiophene)		10^{-1}
Organic–inorganic hybrid	Phenethylamine–tin iodide	~1

Figure 1-4 Comparisons of typical organic and inorganic semiconductors [1].

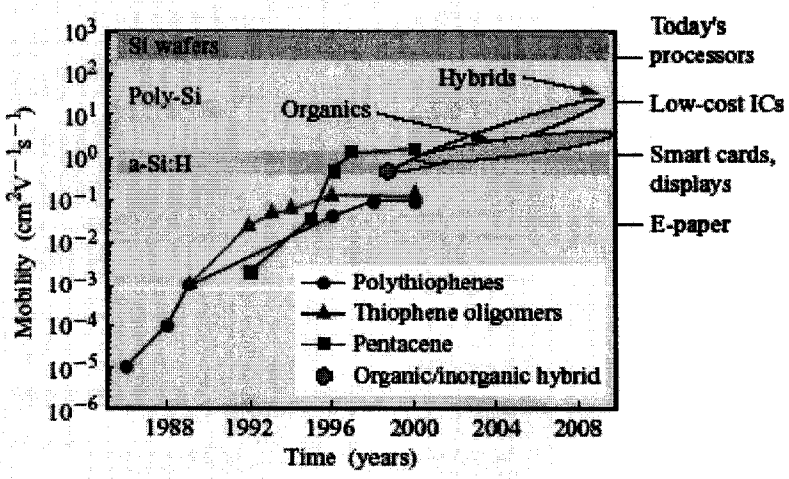


Figure 1-5 Performance of organic and hybrid semiconductors [1].

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1.2 Fabrication and Characterization Techniques

Organic materials including polymers and oligomers can be deposited onto a substrate using various techniques like spin-coating, thermal evaporation, photochemical lithography, ink-jet printing process, screen-printing, micromolding, micro-contact printing (μCP) [12], etc.

1.2.1 Spin-coating

Spin coating is generally regarded as the best way to deposit a uniform coating for many applications such as photoresist coating and insulating layer coating. It gives optimal coverage with minimum material usage. This deposition technique is extremely desirable because the process is simple, safe, and inexpensive. A detailed description of spin-coating technique is demonstrated in literature [13].

1.2.2 Vacuum Thermal Evaporation

The vacuum thermal evaporation technique consists of heating until evaporation of the material is to be deposited. The material vapor finally condenses in the form of a thin film on the substrate surface and on the vacuum chamber walls. Usually, low pressures about 10^{-6} or 10^{-5} Torr are used, to avoid the reaction between the vapor and atmosphere. Small molecular organics can be deposited by thermal vacuum evaporation such as NTCDA and pentacene [14][15].

1.2.3 Ink-jet Printing Process

Ink-jet printing process is a method in which the polymer solution takes the place of the toner in a printer. In this method, the polymer pattern can be directly printed onto the substrate. With this technique, the polymer solution can be applied to the substrate in the size of a pixel, giving very high-resolution patterns and the ability to separate pixels

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of red, green, and blue emitting polymers onto the substrate. Ink-jet printing has been applied to polyvinylcarbazole (PVK)/dye composites using a commercial inkjet printer with 65 μm nozzles [16]. Ink-jet printing has also been used to deposit the conducting polymer to create dual-color light-emitting pixels [17].

1.2.4 Screen-printing and Micromolding

Screen-printing and micromolding are recently used to fabricate functional all-polymer transistors [5][18] with advantages of mass production and transferability. Screen-printing prints patterns by squeezing ink through a predefined screen mask and transferring patterns to the substrate. Micromolding is one type of soft lithography technique to pattern source and drain electrodes.

1.2.5 Micro-contact Printing

The micro-contact printing technique is based on the selective transfer of polymer material to a substrate via a polydimethylsiloxane (PDMS) stamp to obtain desired patterns or exposed and covered regions of the substrate. This can be used for the deposition of polymer materials by area-selected electropolymerization [19] or area-selected deposition [20].

1.3 Mechanisms of Conduction

Organic solids are formed by covalent bonds without electron overlap. There are no significant hole and electron carriers in the traditional sense. The excitations exist on organic molecules in the states of solitons, polarons, and bipolarons [21]. Organic chemistry shows that conjugated double bonds behave quite differently from isolated double bonds. As indicated, conjugated double bonds act collectively, knowing that the next nearest bond is also double [1][2]. Hückel's theory [22] and other simple theories

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predict that π electrons are delocalized over the entire chain and that the band gap becomes vanishingly small for a long enough chain. One reason for this prediction is the character of a π molecular orbital, including the p orbitals of all carbon atoms along the chain of conjugated double bonds. When looking at the distribution of electron density, to which all filled molecular orbitals contribute, the electrons are predicted to be blocked off rather evenly along the entire chain [23]. In other words, all bonds are predicted to be equal. One reason why polyacetylene is a semiconductor and not a conductor is because the bonds are not equal. There is a distinct alternation: every second bond having some double-bond character.

The role of the dopant is either to remove or to add electrons to the polymer. For example, iodine (I_2) will abstract an electron under formation of an I_3^- ion. If an electron is removed from the top of the valence band of a semiconductive polymer, such as polyacetylene or polypyrrole, the vacancy (hole) created does not delocalize completely, as would be predicted from classical band theory. If an electron is removed from one carbon atom, a radical cation will be produced.

The radical cation or anion (polaron) is localized, partly because of Coulomb attraction to its counterion (I_3^-), which is the quasiparticle composed of a single electronic charge dressed with a local geometrical relaxation of the bond lengths [21]. A polaron can be thought of as a bound state of a charged soliton and a neutral soliton whose midgap energy states hybridize to form bonding and antibonding levels. A polaron has normally a very low mobility, partly because of a local change in the equilibrium geometry of the radical cation relative to the neutral molecule [24].

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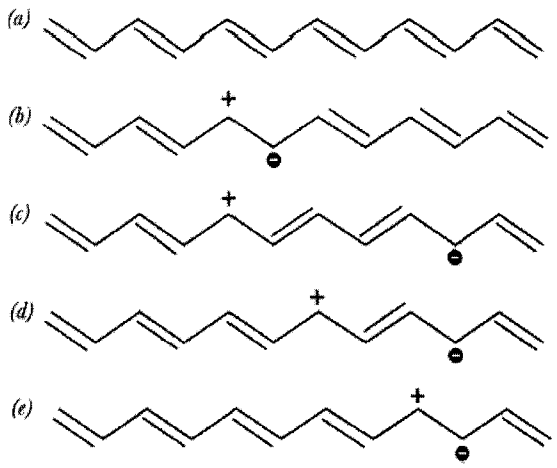

Figure 1-6 Radical cation (polaron) formation and migration [23].

The mobility of a polaron along the polyacetylene chain can be high and charge is carried along as shown in Figure 1-6. Radical cation (polaron) formed by removal of one electron on the 5th carbon atom of an undecahexaene chain (a → b). The polaron migration is shown in c → e [23]. However, since the counterion (I_3^-) to the positive charge is not easy to transport, a high concentration of counterions is required so that the polaron can move in the field of close counterions. This explains why so much doping is necessary.

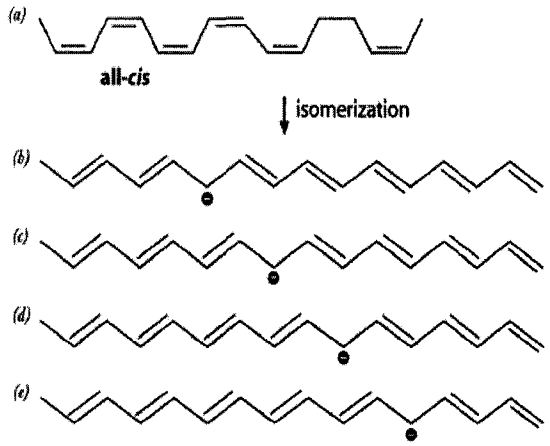

Figure 1-7 Creation and transportation of a soliton [23].

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If a second electron is removed from an already-oxidized section of the polymer, either a second independent polaron may be created or a bipolaron (a bound state of two charged solitons of like charge, or two polarons whose neutral solitons annihilate each other with two corresponding midgap levels [21]) is formed if it is the unpaired electron of the first polaron that is removed [21][23]. The two positive charges of the bipolaron are not independent, but move as a pair, like the Cooper pair in the theory of superconductivity. While a polaron, being a radical cation, has a spin of 1/2, the spins of the bipolaron's sum is S = 0. Other carriers in polymer chain defects which are important for conductivity in polyacetylene are solitary wave defects solitons. Figure 1-7 shows how a cis-polyacetylene chain by undergoing thermal isomerization to trans-structure may create a defect, a stable free radical: this is a neutral soliton which, although it can propagate along the chain, may not carry any charge itself. A soliton is created by isomerisation of cis-polyacetylene (a → b) and moves by pairing with an adjacent electron (b → e) [23]. On the other hand, it may contribute to the charge transfer between different chains.

Bulk conductivity in the polymer material is limited by the need for the electrons to jump from one chain to the next. For example, in molecular terms an intermolecular charge transfers reaction. It is also limited by macroscopic factors such as bad contacts between different crystalline domains and grain boundaries in the material.

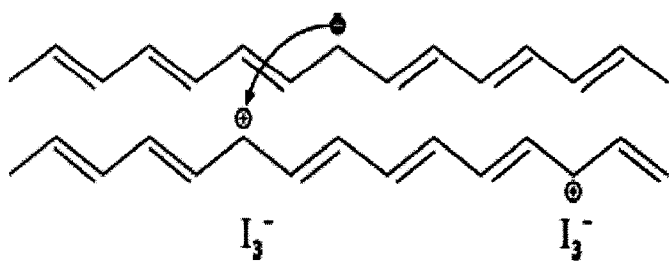

Figure 1-8 Intersoliton hopping and interaction of solitons [23].

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One mechanism proposed to account for conductivity by charge-hopping between different polymer chains is "intersoliton hopping" (Figure 1-8). In intersoliton hopping, charged solitons (bottom in Figure 1-8) are trapped by dopant counterions, while neutral solitons (top) are free to move. A neutral soliton on a chain close to one with a charged soliton can interact: the electron hops from one defect to the other [23]. Here, an electron is jumping between localized states on adjacent polymer chains; the role of the soliton is to move around and to exchange an electron with a closely located charged soliton, which is localized. The mechanism at work in intersoliton hopping is very similar to that operating in most conducting polymers somewhere in between the metallic state at high doping and the semiconducting state at very low doping. All conjugated polymers do not carry solitons, but polarons can be found in most of them. Charge transport in polaron-doped polymers occurs via electron transfer between localized states being formed by charge injection on the chain [25].

1.4 Technology Computer Aided Design (TCAD)

TCAD modeling is the art and science of abstracting a device and electrical behavior of integrated circuit (IC) and supported by critical analysis including detailed understanding based on computer simulations. Specifically, a TCAD tool set has emerged over the last two decades—along with a methodology for its use—that takes input from the IC mask information and specifications of the processing technology and systematically supports development of electrical representations using these "computational prototypes." TCAD models can capture both higher level behaviors as well as provide correlation with the deeper physical (fabrication) details. Figure 1-9 shows schematically this flow of information.

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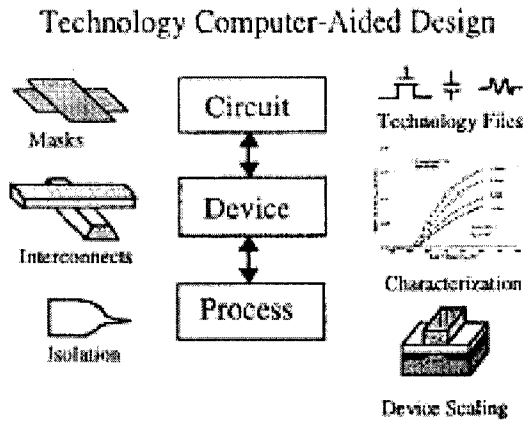

Figure 1-9 Classic TCAD domains and samples of information [26].

The tools that define the TCAD field including process, device and circuit modeling have evolved steadily over the past two decades, moving from research prototypes (both in industry and academia) towards robust workhorse engines that support both research and manufacturing applications. Figure 1-10 shows a schematic timeline of evolution for device simulation, starting with pioneering industrial work at AT&T [27] and IBM [28], leading to major university efforts such as Technical University of Vienna [29] and Stanford University [30], and finally culminating in a rapid growth of TCAD vendors and the development of commercial platforms that support a broad and heterogeneous set of users.

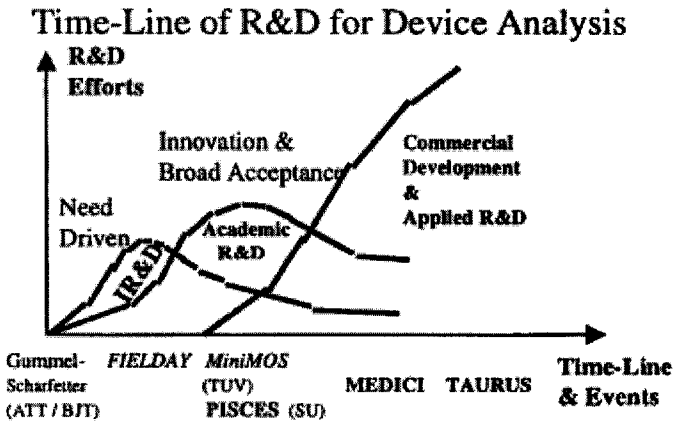

Figure 1-10 Schematic time-line of TCAD R&D for device analysis [26].

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Some of the requirements for TCAD, as viewed from the customer's point, are summarized in Figure 1-11. These views contrast design-driven and technology driven approaches within the microelectronics industry. A growing sector of the industry includes "fabless" integrated circuit (IC) companies that specialize in design. Their intellectual property domain ranges from the system concepts and hardware/software implementations to the supporting design methodologies and value-added tools. The roles for TCAD in this environment are in facilitating predictive extraction of electrical behavior and parameterization of technology dependencies. These capabilities allow scalable reuse of designs, targeting of designs for technology at specific fab, a common language between designers and technologists. On the "megafab" side, the huge capital investment requires the use of TCAD to shorten development cycles and allow targeting of designs for manufacturing, sometimes with a product mix that necessitates flexibility in those targets. Especially in the context of cyclical business trends, such flexibility can be of paramount economic importance. Also shown is the essential supporting infrastructure of equipment suppliers, including metrology and calibration. The complexity of deep submicron technology has led to higher performance requirements for the suppliers, a closer partner relationships, and an increased dependence on "out sourcing" development of generic process modules to the equipment suppliers. TCAD is now playing a significant role on the side of the equipment supplier.

With the investigations and studies of carrier transport mechanism of organic materials, TCAD has been employed to simulate organic devices in the area of microelectronics and optoelectronics since the last decade. TCAD will be important to the development and applications of conducting organics.

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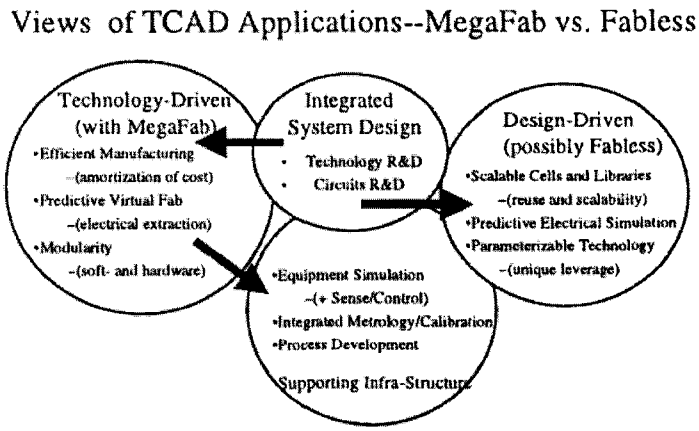

Figure 1-11 TCAD applications in "MegaFab" and "Fabless" environments [26].

1.5 Objectives

The objectives of this project are to fabricate and simulate the organic microelectronic devices by traditional lithography process and Technology Computer Aided Design (TCAD), respectively. In detail:

1. **Fabrication and Characterization.** Several basic device structures will be investigated in this project, which include metal-insulator-metal (MIM) capacitors, metal-insulator-semiconductor (MIS) capacitors, Schottky diodes, and metal-insulator-semiconductor field-effect transistors (MISFETs). A series of novel investigations on temperature dependence of mobility and modification at semiconductor/insulator interface are carried out and discussed.
2. **Modeling and Simulation**. Currently, the modeling and simulation of organic microelectronic devices are very limited due to the unclear mechanisms of electrical transport of organic materials. It is necessary to model and simulate organic devices to study, analyze, and verify the transport mechanisms of organic materials. We will employ TCAD tools MEDICI and Taurus-Device (Synopsys®)

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to simulate the fabricated devices and generate the models based on the experimental results and simulation results.

1.6 Organization of this Dissertation

Chapter One introduces the discovery and development of organic microelectronics, the various applications of conducting and semiconducting organics in microelectronics, fabrication techniques, conduction mechanism, introduction to TCAD, and the objectives of this dissertation. Chapter Two describes the fabrication and characterization of capacitors involving organic insulators and semiconductors. Chapter Three illustrates the construction of Schottky diodes and TCAD simulation. Chapter Four details the design, realization and improvement of organic field-effect transistors (OFETs). Moreover, a detailed TCAD simulation is carried out based on the fabricated devices. The conclusion and the work for future studies are addressed in Chapter Five.

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Table 1-1 List of the abbreviations used in this dissertation.

Abbreviation	Full name
6T	Sexithiophene
BOC	Bottom contact
BOE	Buffered oxide etch
FET	Field-effect transistor
HOMO	Highest occupied molecular orbital
IC	Integrated circuit
IPA	Isopropyl alcohol
ITO	Indium tin oxide
LBL	Layer-by-layer
LED	Light-emitting diode
LUMO	Lowest unoccupied molecular orbital
MEH-PPV	Poly[2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene]
MESFET	Metal-semiconducting field-effect transistor
MIM	Metal-insulator-metal
MIS	Metal-insulator-semiconductor
MISFET	Metal-insulator-semiconductor field-effect transistor
MOS	Metal-oxide-semiconductor
NTCDA	Naphthalene-tetracarboxylic-dianhydride
OTS	Octadecyltrichlorosilane
PDDA	Poly(dimethyldiallylammonium chloride)
PDMS	Polydimethylsiloxane
PPV	Poly(para-phenylene vinylene)
PPy	Polypyrrole
PSS	Poly(styrenesulfonate)
PVK	Polyvinylcarbazole
PVP	Poly(4-vinylphenol)
QCM	Quartz crystal microbalance
RIE	Reactive ion etching
RST	Roughness step tester
S/D	Source and drain
SAM	Self assembled monolayer
SCLC	Space-charge limited conduction
SEM	Scanning electron microscopy
TCAD	Technology computer aided design
TFT	Thin film transistor
TOC	Top contact
μCP	Micro-contact printing

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CHAPTER TWO

ORGANIC CAPACITORS

2.1 Introduction

Capacitors are basic microelectronic components of ICs for wireless communication, memory, etc. Several literatures for organic capacitors consisting of organic insulators [31][32][33] and conducting polymer [34][35][36] are reported. The investigation of organic insulators will benefit the realization of all organic microelectronics. In this project, we focus on the fabrication and characterization of organic insulator. Furthermore, the investigated insulator will be used to construct organic MIS capacitors and FETs involved. The parameters for the MIS capacitors and FETs are calculated with the assistance of the investigated dielectric constant.

2.2 Theory of MIM and MIS Capacitors

2.2.1 Metal-insulator-metal (MIM) Capacitors

A metal-insulator-metal (MIM) capacitor (also known as the parallel-plate capacitor) is one of the most common components in electronics, which is composed by two electrodes sandwiching a layer of insulator. The following equation describes the fundamental behavior of a MIM capacitor,

$$C_0 = \frac{K_I \varepsilon_0}{d} A \qquad (2\text{-}1)$$

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C_0 is the capacitance, K_I is the dielectric constant of the insulator, ϵ_0 is the permittivity of free space, d is the thickness of the insulator (distance between two electrodes), and A is the area of electrodes.

The investigation is based on insulating polymer poly(4-vinylphenol) (PVP) [37], which is a common material as an insulator in organic microelectronics [38][39] and as photoresist in soft lithography [40]. Figure 2-1 shows the molecular structure of PVP. The fabrication and characterization are discussed in Section 2.

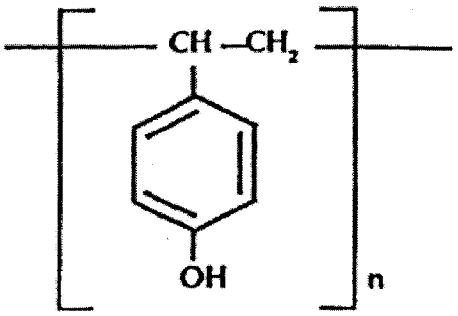

Figure 2-1 Molecular structure of poly(4-vinylphenol) (PVP).

2.2.2 Metal-insulator-semiconductor (MIS) Capacitors

Metal-insulator-semiconductor (MIS) capacitors are usually referred to capacitor structures other than thermal oxide on silicon substrate [41], which form typical Metal-oxide-semiconductor (MOS) capacitors. The structure shown in Figure 2-2 is the basic configuration of MIS capacitor. If the semiconductor is replaced by another layer of metal, it is a typical parallel-plate capacitor, described by Equation 2-1. However, the MIS capacitor is more complicated because of the voltage dependence of the surface space-charge layer in the semiconductor [42]. The space charge of the depletion layer acts as another capacitor C_d in series with C_0, giving an overall capacitance of

$$C = \frac{C_0 C_d}{C_0 + C_d} \tag{2-2}$$

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The capacitance of depletion layer is

$$C_d = \frac{K_s \varepsilon_0}{x_d} \tag{2-3}$$

where K_S is the dielectric constant of the semiconductor and x_d is the thickness of the depletion layer.

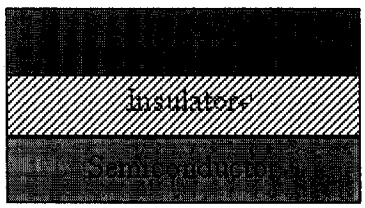

Figure 2-2 Schematic structure of MIS capacitor.

Under the condition of carrier accumulation, there is no depletion layer under the semiconductor surface, and the overall capacitance is equal to C_0. In strong inversion, the maximum space-charge width x_{dm} becomes a constant, and C_d is also a constant. With biasing voltage between the condition of carrier accumulation and strong inversion, the width of the space-charge layer x_d and the capacitance are the function of the bias voltage V_G. Equations 2-4 and 2-5 give the calculation of x_d and the capacitance in the high frequency bias voltage [42],

$$x_d = \frac{K_S \varepsilon_0}{C_0}\left(\sqrt{1+\frac{2V_G}{qK_S\varepsilon_0 N_a}C_0^2}-1\right) \tag{2-4}$$

$$C = \frac{C_0}{[1+(2C_0^2/qN_aK_S\varepsilon_0)V_G]^{1/2}} \tag{2-5}$$

where N_a is the doping concentration of semiconductor.

The maximum width of depletion region is calculated by [42],

$$x_{dm} = \sqrt{\frac{2K_S\varepsilon_0\phi_s}{qN_a}} = \varepsilon_0 K_S\left[\frac{1}{C_{\min}}-\frac{1}{C_0}\right] \tag{2-6}$$

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where C_{min} is the minimum capacitance and surface potential ϕ_s is,

$$\phi_s = 2\phi_f + 6\phi_T \tag{2-7}$$

as the condition of the onset of strong inversion of carrier. ϕ_f is the difference between the midgap E_i and the Fermi level E_f in the bulk of the semiconductor,

$$\phi_f = \phi_T \ln(\frac{N_a}{n_i}) \tag{2-8}$$

with $\phi_T = kT/q$. Since kT represents the thermal energy at temperature T, ϕ_T is considered as the voltage equivalent of temperature. k is the Boltzmann's constant and n_i the intrinsic carrier concentration of the semiconductor. An energy band diagram of the MIS capacitor is shown in Figure 2-3.

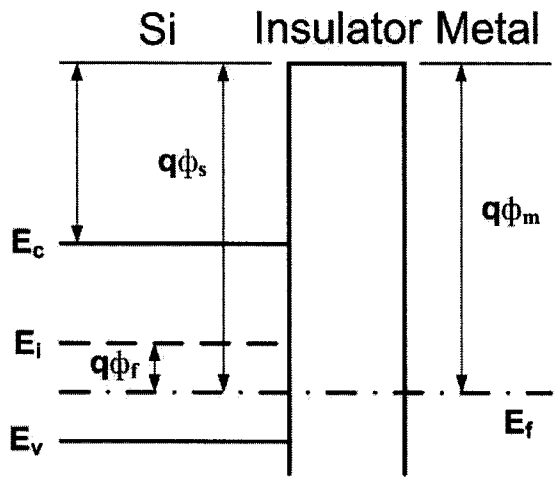

Figure 2-3 Energy band diagram of the MIS capacitor at thermal equilibrium.

Capacitance-voltage characteristics can be employed to determine the doping concentration in the semiconductor [43],

$$N_a(x_d) = \frac{-2\Delta V_G}{q\varepsilon_0 K_S A^2 \Delta(1/C^2)} \tag{2-9}$$

More detailed descriptions of MIS capacitor can be found in [42][43][44].

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2.3 Capacitors with Organic Insulator

2.3.1 Design and Fabrication

A vertical structure of MIM capacitor is shown in Figure 2-4(a). Two layers of aluminum (Al) are the electrodes in this device, which sandwich a layer of insulating polymer PVP. The detailed fabrication steps are:

(1) Evaporate a layer of Al (1500Å) on silicon substrate;

(2) Spin on a layer of PVP (2% in isopropyl alcohol (IPA)) (4000 Å);

(3) Evaporate another layer of Al (1500Å);

(4) Define the pattern on the top Al layer by lithography;

(5) Etch the top Al;

(6) Remove the photoresist by acetone;

(7) Using oxygen reactive ion etching (RIE) to etch PVP and expose the bottom layer Al (the top Al acts as mask).

The bottom layer can be replaced by Cu or Au to avoid the effects from the patterning of the top Al layer. A microscopic picture of a real fabricated device is shown in Figure 2-4(b) (top view) with a dimension of 800 μm by 800 μm. The oxygen RIE may cause the degradation of the polymer, which is not characterized in this project.

2.3.2 Characterization and Discussion

The capacitance-voltage (C-V) characteristics are measured by the Keithley Test Station (Model 82-WIN). The typical result is shown in Figure 2-5 from low-frequency (by the quasi-static technique [43]) measurement. The ideal capacitance of MIM capacitor should be a constant. In our investigations, the capacitance varies with the applied voltage, which is caused by non-uniformity of insulating thin film and top-layer

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Al. The thickness of PVP is measured to be 400 nm by the Roughness Step Tester (RST). Therefore the dielectric constant can be carried out to be about 5.6 by Equation 2-1 and the mean value of the capacitance.

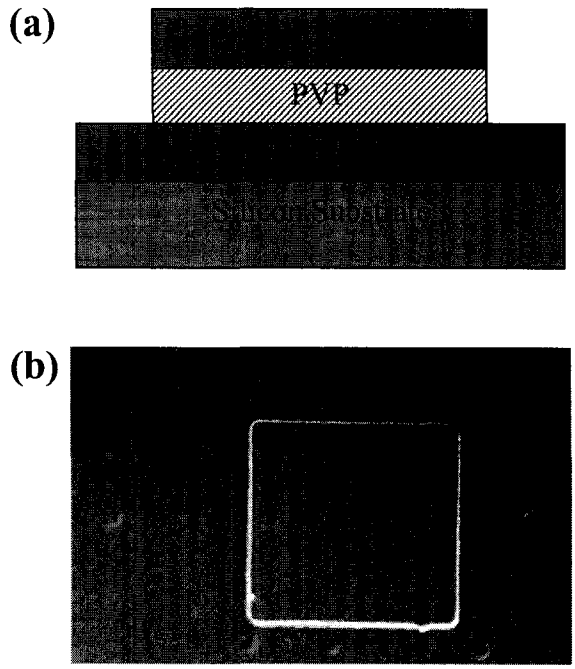

Figure 2-4 A fabricated MIM capacitor: (a) schematic structure and (b) micrograph.

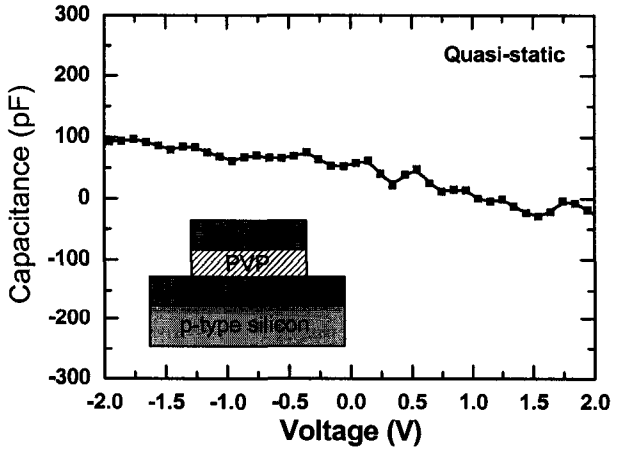

Figure 2-5 C-V characteristics of MIM capacitors with PVP at low frequency.

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2.3.3 Verification

In order to verify the former results, a MIS capacitor was fabricated with PVP as an insulator and the silicon (p-type) as the semiconductor. A schematic structure is shown in the inset of Figure 2-6. The methods of fabrication are similar to the MIM capacitor: (1) spin-coating of the PVP on silicon substrate; (2) evaporation of the Al layer; (3) lithography of the Al layer; (4) Removal of photoresist; and (5) the RIE etching of the PVP. The typical high frequency capacitance characteristics are shown in Figure 2-6, and the results of the fabricated devices are summarized in Table 2-1. Dielectric constants are calculated from the accumulation region according to Equation 2-1.

Table 2-1 Results for fabricated Al-PVP-Si capacitors.

	Area (μm*μm)	Thickness (nm)	Capacitance (pF)	k
Sample 1	200*200	113	19.7	6.3
Sample 2	350*350	110	60.4	6.1
Sample 3	500*500	118	115.0	6.1
Sample 4	550*550	117	128.0	5.6
Sample 5	700*700	120	205.0	5.6

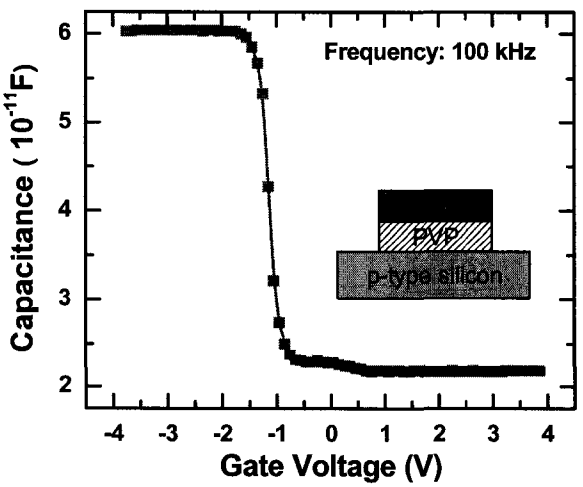

Figure 2-6 Capacitance-voltage characteristics of Al-PVP-Si capacitors at 100 kHz.

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The values of the dielectric constant range from 5.6 to 6.3, which are consistent with the former results from Al-PVP-Al structure, about 5.6. The mean value and standard deviation of dielectric constants are 5.94 and 0.32, respectively, in the aspect of statistics for the data in Table 2-1. This result is more trustable than what we carried out in the last section because of a fewer fabrication steps are involved and the capacitance curves are more stable.

2.4 Capacitors with Organic Semiconductor

2.4.1 Design and Fabrication

A similar structure is used to fabricate metal-insulator-semiconductor (MIS) capacitors, as shown in Figure 2-7. In this structure, highly doped n-type silicon serves as the substrate and bottom electrode. PVP serves as an insulator. Pentacene is a p-type organic semiconductor, which is widely investigated in organic microelectronics. The molecular structure of pentacene is shown in Figure 2-8. Ti and Au layers are sputtered on pentacene as the top electrode. The fabrication procedure is,

1. Spin-coating of the PVP (2% solution in IPA) (about 120-130 nm) on ITO/Glass substrate;
2. Thermal evaporation of pentacene (about 70-80 nm);
3. Sputtering Ti and Au (about 30 nm and 80 nm);
4. Lithography to define the pattern of Ti and Au;
5. Etching of Au and Ti with the KI solution and the buffered oxide etch (BOE) solution, respectively;
6. Removal of photo resist by acetone;
7. Patterning of PVP and pentacene by oxygen RIE, top Ti and Au as mask.

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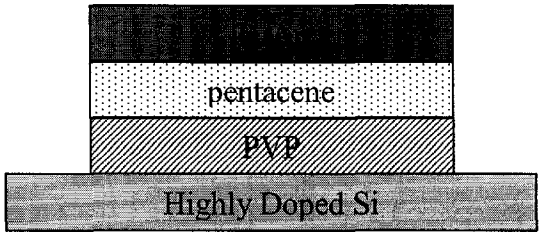

Figure 2-7 Schematic structure of MIS capacitors with organic semiconductor.

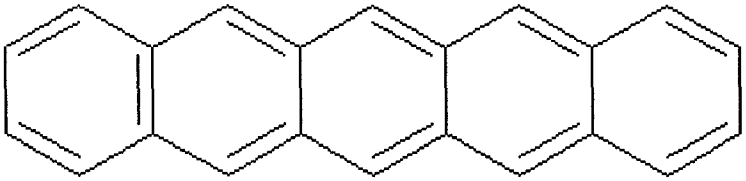

Figure 2-8 Molecular structure of pentacene.

2.4.2 Characterization and Discussion

Structures of the energy band of Si/PVP/pentacene at equilibrium and under applied voltage are shown in Figure 2-9. At equilibrium, Fermi levels of all materials align, as demonstrated in Figure 2-9(a). When a negative voltage is applied over Si/PVP/pentacene, the resulting negative surface potential produces an upward bending of the energy-band diagram, and positive carriers form an accumulation region near the PVP/pentacene interface, shown in Figure 2-9(b). When a positive voltage is applied through Si/PVP/pentacene, the surface is positively charged and the energy bands bend downward, as demonstrated in Figure 2-9(c). The Fermi level near the PVP/pentacene interface is now farther away from the Highest Occupied Molecular Orbital (HOMO), indicating a smaller density of positive carrier, and a depletion region is established at that interface. The calculated maximum width of the depletion region is around 18.5 nm, according to Equation 2-6.

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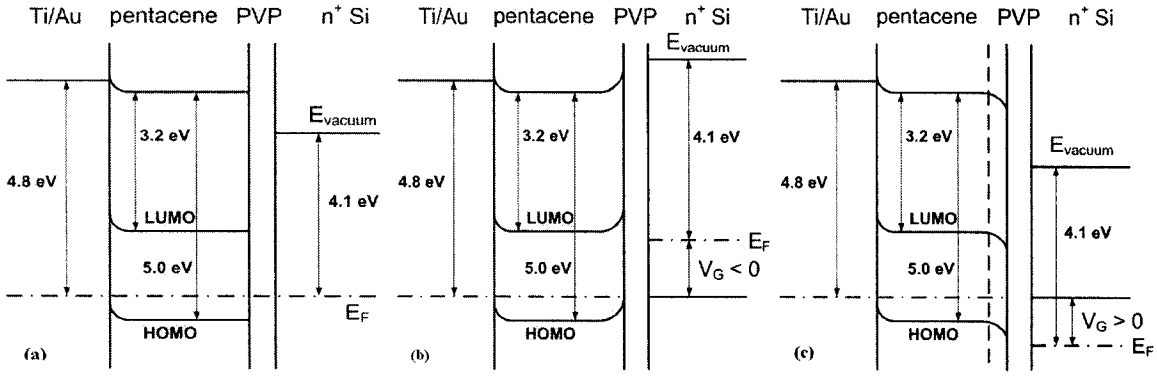

Figure 2-9 Energy band of pentacene MIS capacitors.

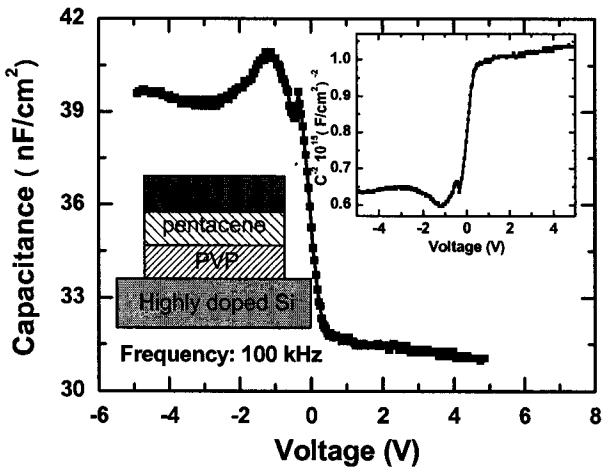

Figure 2-10 C-V characteristics of metal-PVP-pentacene structure at high frequency.

The Capacitance-Voltage characteristics of the Si/PVP/pentacene capacitor, at high frequency (100 kHz), are shown in Figure 2-10, with C^{-2}-V plot inserted. At the linear region near zero bias voltage, the calculated effective carrier density is 8.1×10^{16} cm^{-3} at room temperature by Equation 2-9. The non-linear region of the C-V characteristics demonstrates the non-uniform distribution of concentration in the pentacene due to the interface state, the irregular surface profile, and the voltage dependent leakage current through the MIS structure.

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CHAPTER THREE

ORGANIC SCHOTTKY DIODES

3.1 Introduction

Poly[2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene]) (MEH-PPV) is a poly(para-phenylene vinylene) (PPV) derived p-type polymer which is among the most popular materials used to build OTFTs and OLEDs [51][52][53]. The molecular structure of MEH-PPV is shown in Figure 3-1. Several studies have been carried out for Schottky diodes by MEH-PPV and various metals [54][55][56]. The characteristics of Schottky contact between polymer and metal are important to investigate both material properties and interface characteristics. The temperature and electric field dependent mobility of MEH-PPV was studied in the literature [57][58].

However, the mobility behavior of MEH-PPV above room temperature has not been reported to our knowledge. In this work, experimental and theoretical efforts have been carried out to investigate the mobility behavior above room temperature, based on the current density-voltage (J-V) characteristics and capacitance-voltage (C-V) characteristics of ITO/MEH-PPV/Al Schottky diodes. The highest mobility is obtained at about 353 K. The space-charge limited conduction (SCLC) model [59] and the field-dependent relationship have been employed to extract mobility values. The value of the effective hole density has been determined to be 2.24×10^{17} cm^{-3}.

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Based on the investigation on the temperature dependence of mobility, the highest mobility value of 0.013 cm^2/Vs has been obtained at 353 K among those carried out at different temperatures in our experiments.

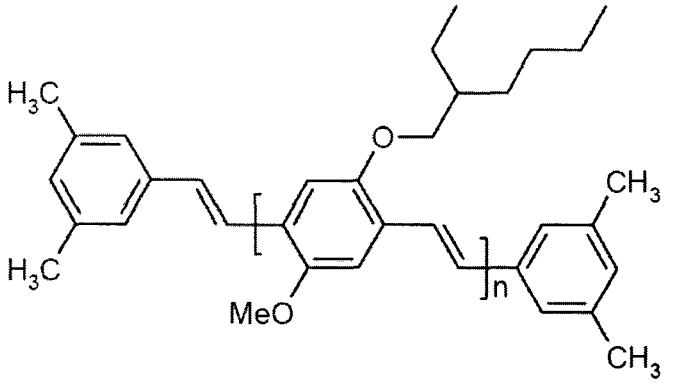

Figure 3-1 Molecular structure of MEH-PPV.

3.2 Device Mechanisms and Models

The SCLC model [57][59] has been widely used to describe the behavior of organic diodes. However, the SCLC model is limited for low electric field (less than 10^5 V/cm) conditions. With the increase in electric field, the SCLC model ignores the field-dependent mobility. Thus, the field-dependent relationship is used to describe accurately the behavior of devices at high electric fields. The classical model [42][43] which normally describes inorganic metal-semiconductor contact is also given to analyze the behavior of devices.

3.2.1 Space-charge Limited Conduction Model

SCLC model was proposed for the bulk transport dominated conduction processes in OLEDs [60], which describes the current limited by the space charge. In other words, the density of free carriers injected into the active region is larger than the number of acceptor levels (assumed p-type material). For organic materials, the SCLC model is

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expected to be applicable due to relatively small acceptor density and small mobility of the carriers. The model is described by the following equation:

$$J = \frac{9}{8}\varepsilon_0\varepsilon_r\mu_p\frac{V^2}{L^3} \tag{3-1}$$

where J is the current density, V is the voltage, $\epsilon_0\epsilon_r$ is the permittivity of the polymer, μ_p is the hole mobility (assumed p-type conducting polymer), and L is the device thickness.

The SCLC regime occurs when the equilibrium charge concentration (before charge injection) is negligible compared to the injected charge concentration. This will form a space charge region near the injecting electrode with the concentration of the space charge rapidly ending away from the electrode. In this space charge regime, the current is proportional to the square of the electric field.

3.2.2 Field-dependent Relationship

Field-dependent models are used to describe the hole mobility in MEH-PPV when the electric field is high (larger than 10^5 V/cm), and the constant mobility in the SCLC model is no longer applicable. The characteristics of current density versus voltage can be described by the equation:

$$J = p(x)e\mu_p[E(x)]E(x) \tag{3-2}$$

with the field-dependent mobility given by

$$\mu_p(E) = \mu_p(0)\exp(\gamma\sqrt{E}) \tag{3-3}$$

where the zero field mobility is given by

$$\mu_p(0) = \mu_0\exp(-\frac{E^*}{k_BT}) \tag{3-4}$$

and

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$$\gamma = B(\frac{1}{k_B T} - \frac{1}{k_B T_0}) \tag{3-5}$$

and where p(x) is the density of the hole concentration at position x, E(x) is the electric field at position x, μ_0 is a constant prefactor, E^* is the activation energy, and T_0 and B are material constants which are equal to 600 K and 2.9×10^{-5} eV(m/V)$^{1/2}$ for MEH-PPV, respectively [57].

3.2.3 Classical Model

When a forward bias voltage is applied, the potential barrier from the semiconductor to metal is reduced which favors the carrier transport from the semiconductor to the metal. The current is described in [43],

$$I = I_0\left[\exp\left(\frac{V - I\cdot R_s}{n\phi_T}\right) - 1\right] \tag{3-6}$$

and

$$I_0 = AA^{**}T^2\exp\left(\frac{-\phi_b}{\phi_T}\right) \tag{3-7}$$

where A is the junction area, A** is the Richardson constant, T is the temperature in Kelvins, R_s is the series resistance, ϕ_T is the thermal voltage at certain temperature which is equal to kT/q, ϕ_b is the barrier height, n is the ideality factor, and I_0 is the reverse saturation current.

3.3 Fabrication Approach

MEH-PPV (American Dye Source, Inc.) 0.2% wt solution was prepared on tetrahydrofuran. Glass substrate is covered by a deposited layer of ITO thin film (60 Å). After substrate cleaning by acetone and deionized water, MEH-PPV was deposited on the

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ITO/glass substrate by the spin-coating technique. After baking at 200°C for 20 minutes, a 200 nm layer of Al was deposited on MEH-PPV through thermal evaporation at a pressure of 1×10^{-6} Torr. Subsequently, the Al and MEH-PPV were patterned by photo lithography and Reactive Ion Etching (RIE) technique using the same mask. Thus, Schottky diodes were formed with ITO as the bottom electrode, Al as the top electrode, and MEH-PPV as the active material. The thickness of MEH-PPV is 200 nm (tested by Tencor Alphastep 500 Surface Profiler). Figure 3-2 shows the fabrication procedure used and the structure of the MEH-PPV based diodes as shown in Figure 3-2(e).

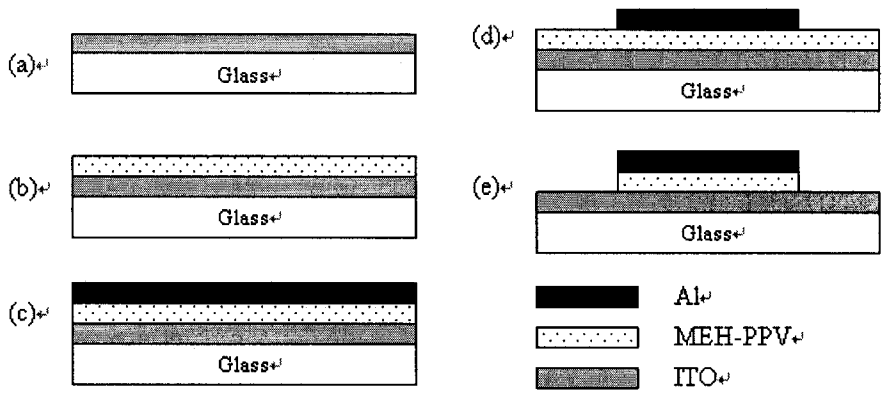

Figure 3-2 Fabrication steps of the MEH-PPV based Schottky diodes.

The Keithley Test Station (236 source measure unit with H1001 heat control module and 590 C-V analyzer) was used to test the fabricated devices from 300 to 400 K. At different temperatures, J-V and C-V characteristics were measured for the fabricated devices and the key parameters such as mobility and carrier density were calculated.

3.4 Electrical Characteristics

3.4.1 Temperature Dependence of Mobility

MEH-PPV and Al form Schottky contact at their interface and generate a depletion region in MEH-PPV, as shown in Figure 3-3 [61]. When a forward voltage is

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applied, the barrier height at the interface decreases when turning on the device. At reverse voltage, the barrier height increases to block the current. The J-V characteristics at different temperatures are shown in Figure 3-4. The J-V^2 characteristics at forward voltage are provided in Figure 3-5 for 325 K, 353 K and 385 K, showing both the experimental (dot) and theoretical (solid line) results. The theoretical results have been calculated from the SCLC model (Equation 2-1, using the thickness of MEH-PPV is 200 nm and assuming the dielectric constant of MEH-PPV is 3 [57]). These results match well with the experimental data at low electric field conditions. With the increase in electric field, the SCLC model underestimates the hole mobility in MEH-PPV, by ignoring the high field effects, which may be described in Equation 3-3.

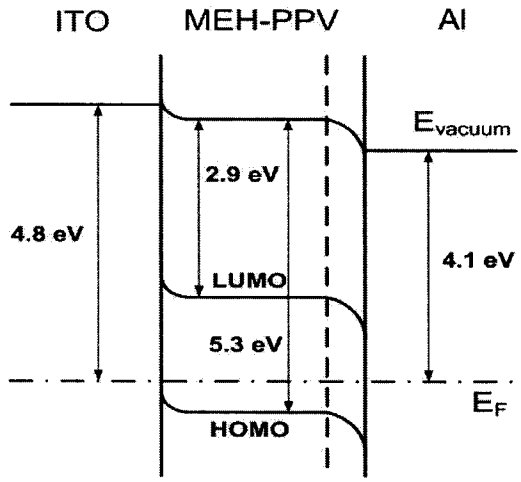

Figure 3-3 Energy-band alignment of the ITO/MEH-PPV/Al structures.

The mobility-temperature plot extracted from the SCLC model at low electric field (10^3 V/cm – 10^5 V/cm) is shown in Figure 3-6. The hole mobility of MEH-PPV increases from 300 to 350 K, which fits the exponential relation in Equation 3-4. Above 350 K, the mobility drops to a lower value, which is attributed to the degradation of MEH-PPV as a conducting polymer, and the increase in carrier scattering happens with the rise in temperature. When the temperature is lowered back, almost the same J-V

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characteristics are measured, demonstrating that no annealing effect exists. The behavior of hole mobility in the regime when it increases with temperature can be exponentially described by Equation 3-4, with the values of μ_0 and E^* determined to be 4.13×10^{-9} cm^2/Vs and 0.451 eV with Equation 3-4, respectively.

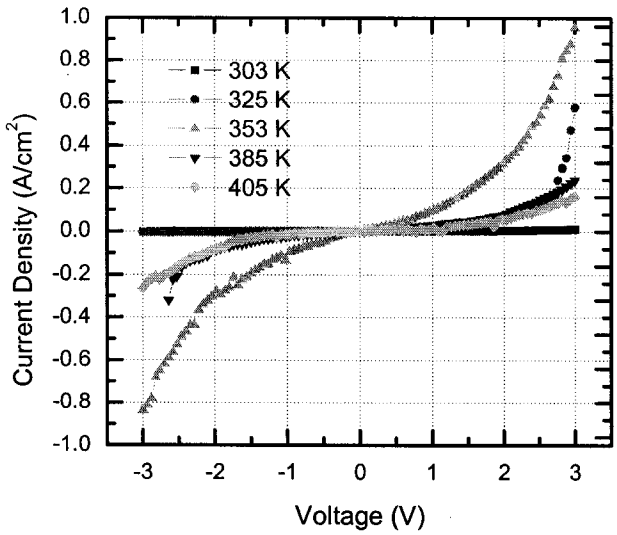

Figure 3-4 J-V characteristics of ITO/MEH-PPV/Al Schottky diodes with temperature.

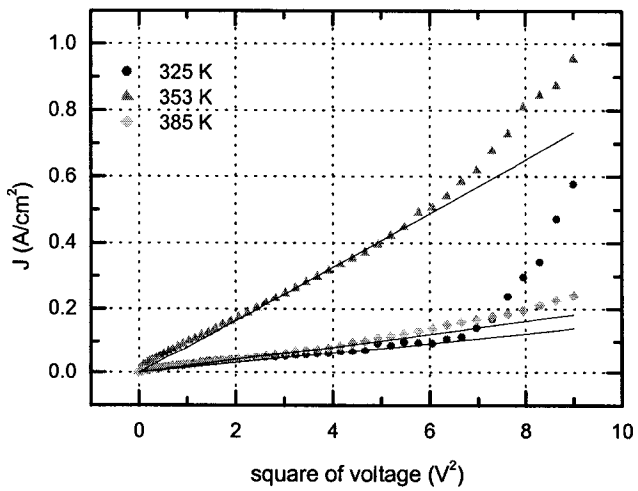

Figure 3-5 J-V^2 characteristics of ITO/MEH-PPV/Al diodes at $V_{ITO/Al} > 0$ V.

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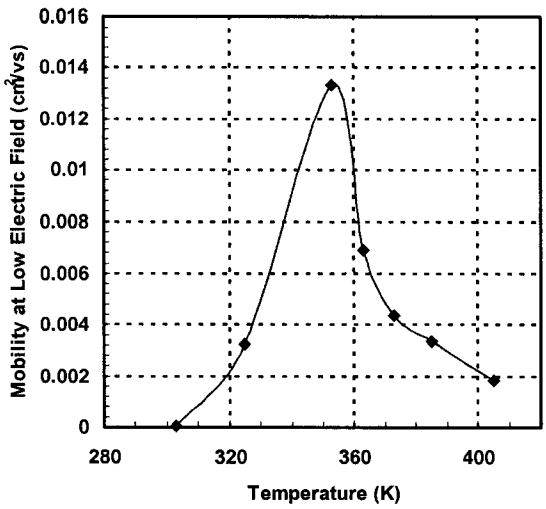

Figure 3-6 Extracted hole mobility in MEH-PPV as a function of temperature.

If $V >> I \cdot R_s$ and $V >> \phi_T$, Equation (3-6) can be rewritten to

$$I = I_0\left[\exp\left(\frac{V}{n\phi_T}\right)\right] \tag{3-8}$$

or

$$\log(I) = \frac{V}{2.3n\phi_T} + \log(I_0) \tag{3-9}$$

The ideality factor and reverse saturation current can be extracted from log(I) vs V relations. Similarly, we can rewrite Equation 3-6 to

$$V = n\phi_T \ln(1 + \frac{I}{I_0}) + I \cdot R_s \tag{3-10}$$

Assuming $I/I_0 >> 1$, and differentiating with respect to I, we get

$$I\frac{dV}{dI} = n\phi_T I_0 + I \cdot R_s \tag{3-11}$$

The series resistance can be extracted from I(dV/dI) vs I relations. The temperature dependencies of reverse saturation current, ideality factor, and series resistance are shown in Figure 3-7. The reverse saturation current shows the same trend

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as mobility. The ideality factor reaches its minimum 4.8 at 325 K, and then goes to a stable value around 6.7. The series resistance decreases with the increase of temperature, which demonstrates proportional relationship between resistivity and temperature for MEH-PPV.

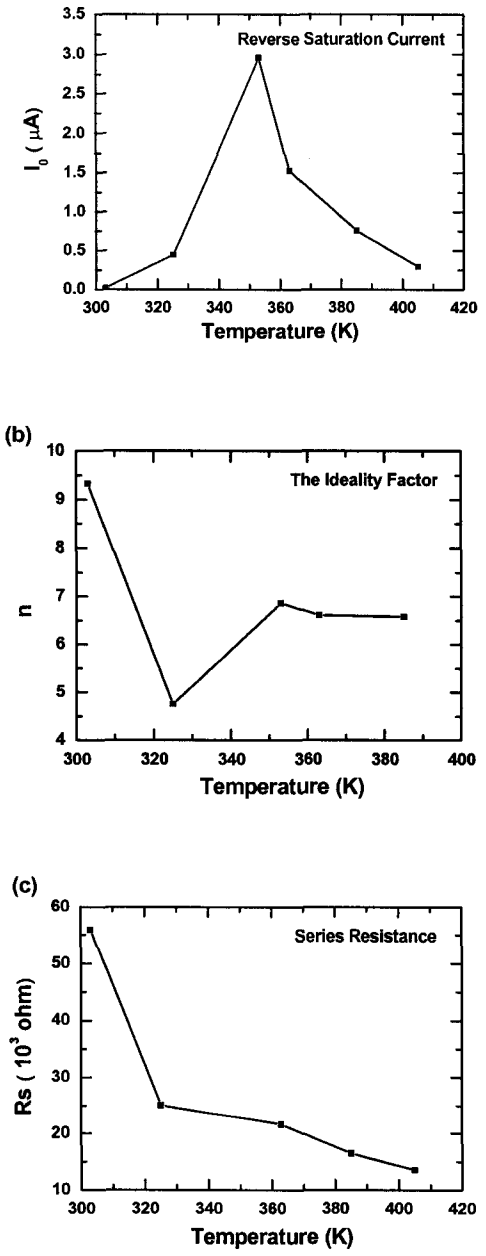

Figure 3-7 Temperature dependence key parameters of Schottky diodes.

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3.4.2 Device Performance

As shown in Figure 3-4, the device performance starts degrading at about 350 K, though a higher mobility is reached. At higher temperatures, the leakage current becomes very large and the device acts more like a resistor instead of a diode. Figure 3-8 shows the detailed plot of J-V characteristics at 325 K, as an example, where significant mobility is obtained as well as relatively lower leakage current. The best ideality factor of 4.8 is obtained at 325 K, according to the classical model which describes the behavior of Schottky diodes under forward bias. At other temperatures, ideality factor is much higher, 7.0 at 353 K, for example. This suggests that the optimal operating temperature of fabricated Schottky diodes is around 325 K with respect to the leakage current and diode behavior, though the highest mobility is not obtained at this point. Compared to the ideality factor for inorganic semiconductors, for example, 1.02 for silicon diodes [42], the ideality factor of MEH-PPV is much larger due to the high resistivity of the organic material.

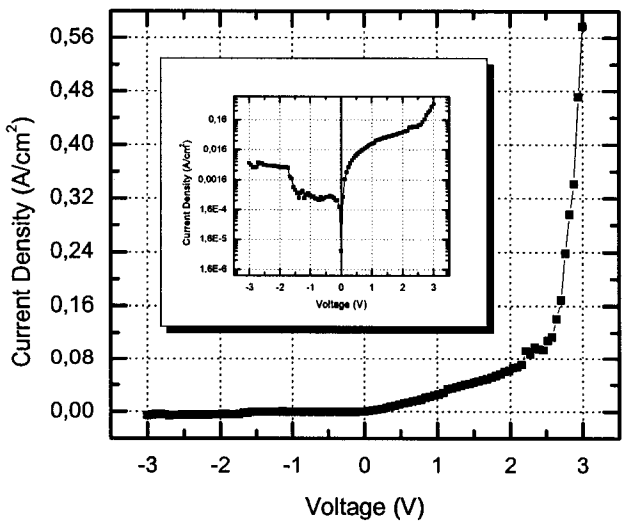

Figure 3-8 J-V characteristics of ITO/MEH-PPV/Al diodes at 325 K.

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Another factor affecting the device performance is the thickness of the active layer. As shown by the J-V curves in Figure 3-9, there is noticeable difference between the two devices considered: one with 70 nm and the other with 200 nm thick layer of MEH-PPV, measured at room temperature. The performance of the 70 nm MEH-PPV device appears much better than that of one with 200 nm MEH-PPV due to the lower resistance.

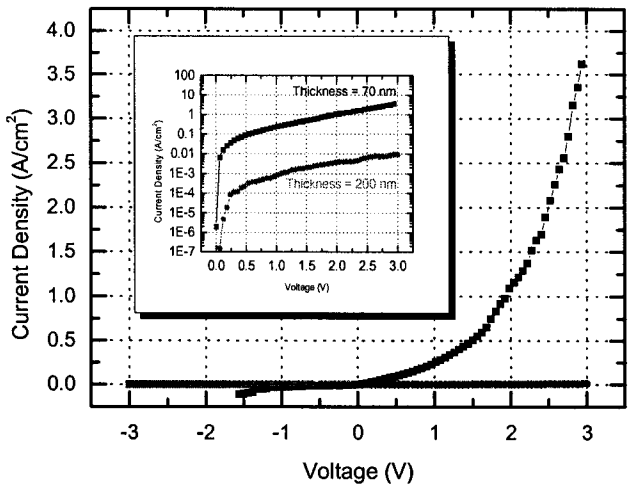

Figure 3-9 J-V characteristics of ITO/MEH-PPV/Al diodes with film thickness.

3.4.3 Charge Distribution

Capacitance-Voltage measurements allow extraction of the effective carrier density and barrier height in the given devices. Equation 2-9 is normally used to extract the carrier density in solid materials and we rewrite it here:

$$N = \frac{-2\Delta V}{q\varepsilon_0\varepsilon_r A^2 \Delta(1/C^2)} \tag{3-7}$$

where N is the carrier density and A the device area.

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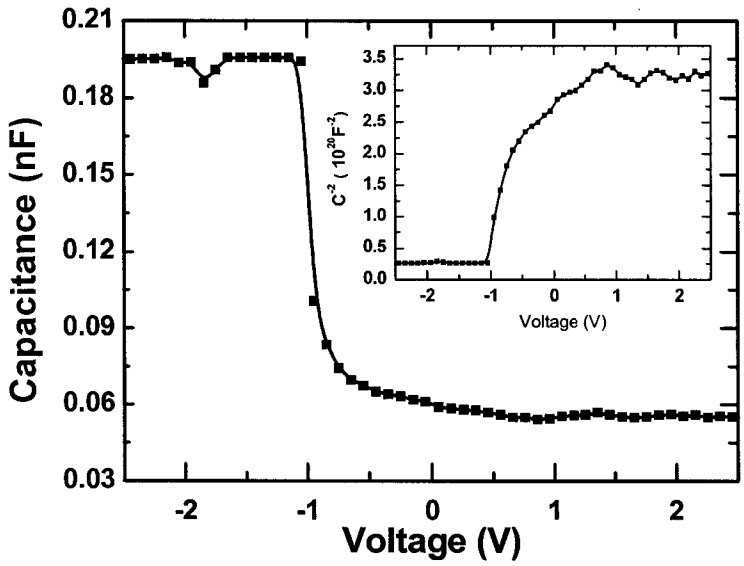

Figure 3-10 C-V Characteristics of ITO/MEH-PPV/Al diodes at high frequency.

Capacitance-Voltage characteristics of the ITO/MEH-PPV/Al diode, at high frequency (100 kHz), are shown in Figure 3-10, with the C^{-2}-V plot inserted. In the linear region near zero bias voltage, the calculated effective carrier density is 2.24×10^{17} cm^{-3} at room temperature and in good agreement with the findings in the literature [63]. The non-linear region of the C^{-2}-V characteristics demonstrates non-uniform distribution of concentration in the MEH-PPV and the presence of interfacial and bulk traps [64]. Assuming that the mobility-independent trap level is 1×10^{21} cm^{-3} [61], the barrier height can be estimated [58][65] at room temperature with the assumption of the difference of work function and the Highest Occupied Molecular Orbital (HOMO) level.

3.5 Modeling and Simulation

Electrical characteristics of organic diodes have been simulated by the traditional drift-diffusion model [66][67][68] or other modified models [57][61]. In our investigation,

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the two-dimensional device simulator Medici [69] is employed to simulate the fabricated device at room temperature. From the analysis in the last section, we notice that the fabricated devices are described well by the SCLC model and the relationship of field dependence. Though Medici (Synopsys®) is a drift-diffusion based simulator, we can identify the factors and parameters which affect the behaviors of the fabricated device to some extent by the numerical simulations.

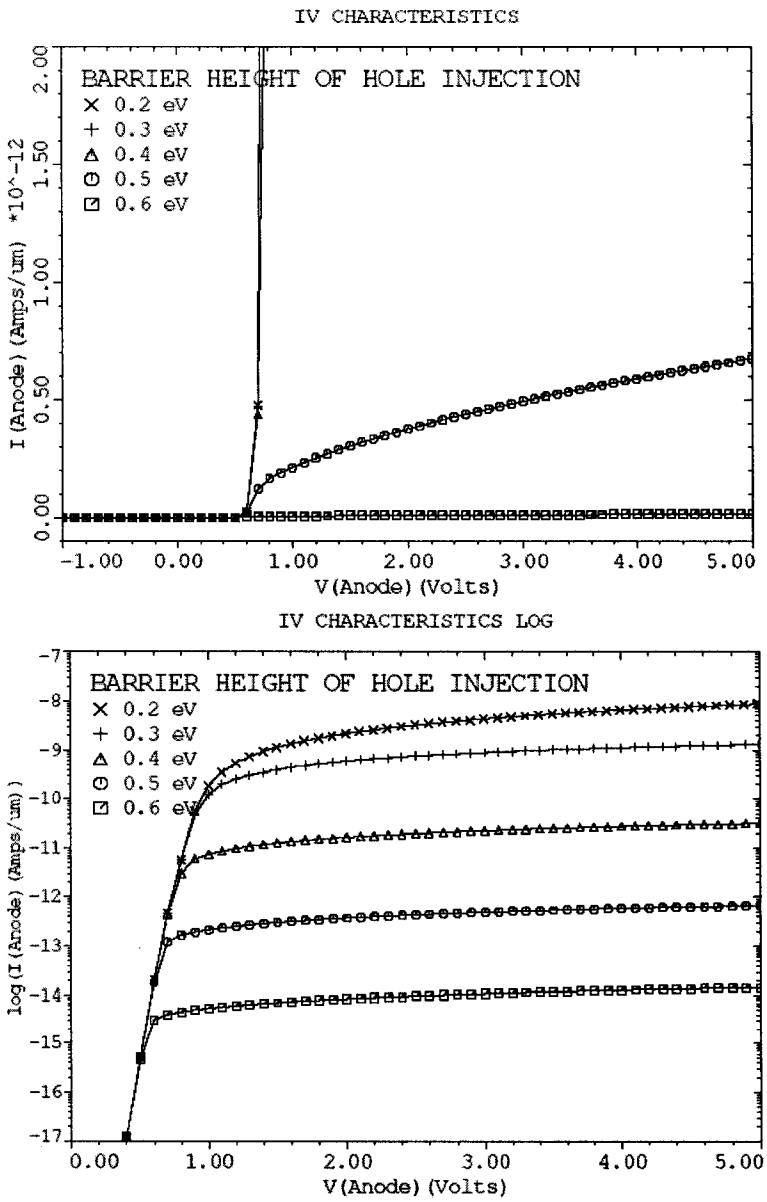

Figure 3-11 I-V behavior of MEH-PPV Schottky diodes with hole injection.

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The main influence of material parameters on the electrical characteristics of organic diodes came from the large energy gap and low mobility. In our simulation, parameters for MEH-PPV are taken with a dielectric constant at 3, with the density of states at 1×10^{21} cm^{-3}, E_C at 2.7-3.0 eV, E_g at 2.1-2.5 eV [61][70][71][72], hole mobility at 6×10^{-5} cm^2/Vs, and doping concentration at 3×10^{17} cm^{-3} from our calculation above. The parameters of geometry are taken from the fabricated devices as well. A typical simulation input file is shown in Appendix A.

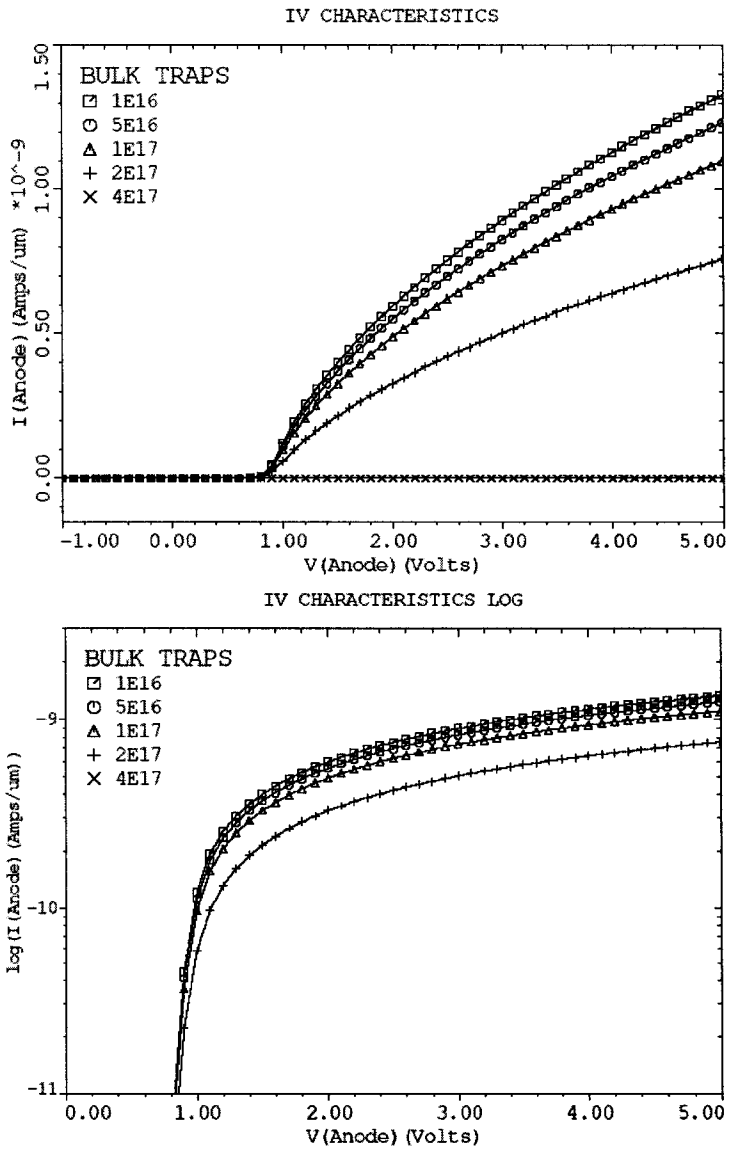

Figure 3-12 I-V behavior of MEH-PPV Schottky diodes with bulk traps.

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Al is the material of cathode and its work function is 4.1-4.3 eV. ITO serves as an anode whose work function varies in a wide range, typically from 4.7 eV to 5.1 eV [55][61][73][74]. Figure 3-11 (linear upper and logarithm lower) shows the I-V characteristics of the device with different work function of the anode, from 4.7 eV to 5.1 eV, corresponding to barrier of the hole injection from 0.6 eV to 0.2 eV according to E_v at 5.3 eV. The simulation results are almost the same for 0.2 eV to 0.4 eV barrier heights. The current flow is limited by the space charge for these cases with small barriers for the hole injection. As the barrier for the hole injection is further increased, the current is decreased rapidly, indicating that the current is limited by the injection.

The bulk traps within semiconducting polymer also limit current flow. Figure 3-12 shows the I-V characteristics of the device with increasing bulk traps. We notice that when the traps are small compared to the hole density in MEH-PPV, its effect is negligible. As traps increase to near the doping concentration, the current flow decreases dramatically due to significant trapping.

By adjusting the work function of the anode and the amount of bulk traps, Figure 3-13 shows a comparison of I-V characteristics between simulation and measurement. The hole injection from ITO is chosen to be 0.3 eV for the barrier height, E_c is 2.8 eV, E_g is 2.2 eV, and bulk traps are chosen to be 3×10^{17} cm^{-3}. Simulation results match experimental results well at higher forward voltage when the device turns on. At the region near zero voltage, a little difference exists due to different conduction mechanisms. With reverse voltage, a measured device shows large leakage current which is not simulated here.

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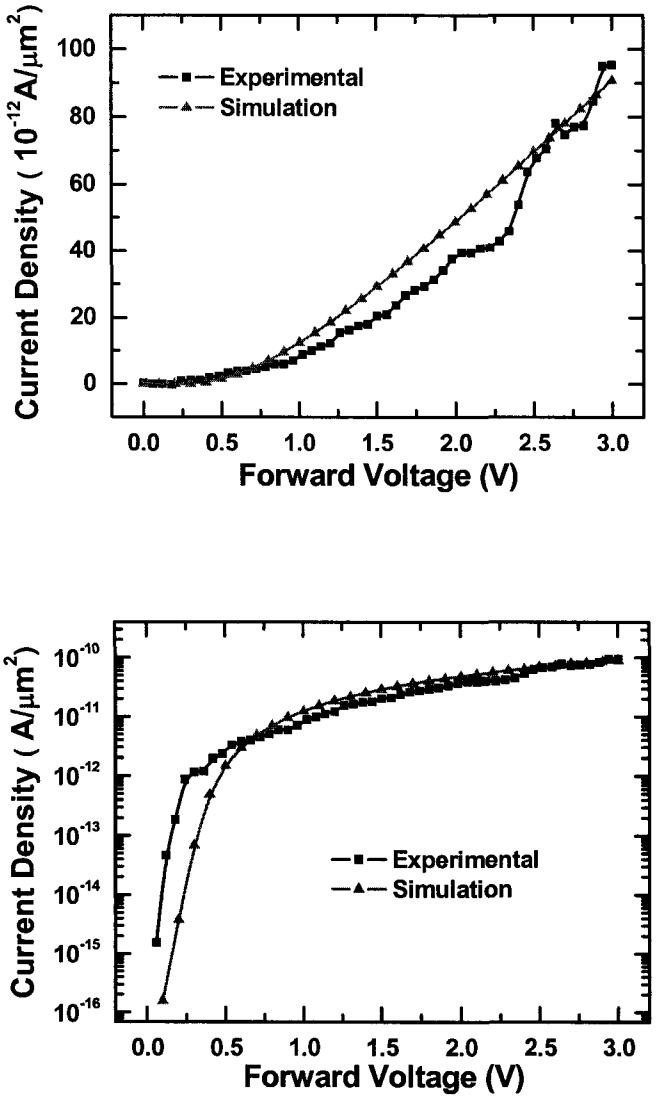

Figure 3-13 Comparison of experimental and simulation results with forward bias.

Figure 3-14 shows the distribution of holes from cathode to anode with different voltages applied to the structure with fitted parameters. We find that higher forward bias helps to release the trapped holes. Figure 3-15 shows the distribution of the electric field from cathode to anode. Large electric field is located at the depletion region of Schottky diode near the cathode. From the simulation results, we find a lower barrier height of hole injection and lower bulk traps are necessary to obtain high performance organic Schottky

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diode. Due to different conduction mechanisms and ultra high resistivity of semiconducting polymer, discrepancy exists between simulation and experimental.

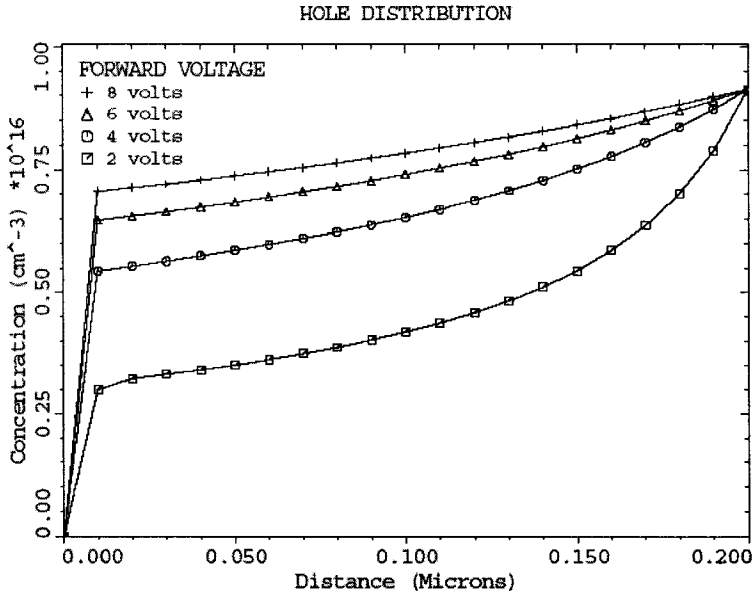

Figure 3-14 Hole density from cathode to anode with different forward bias.

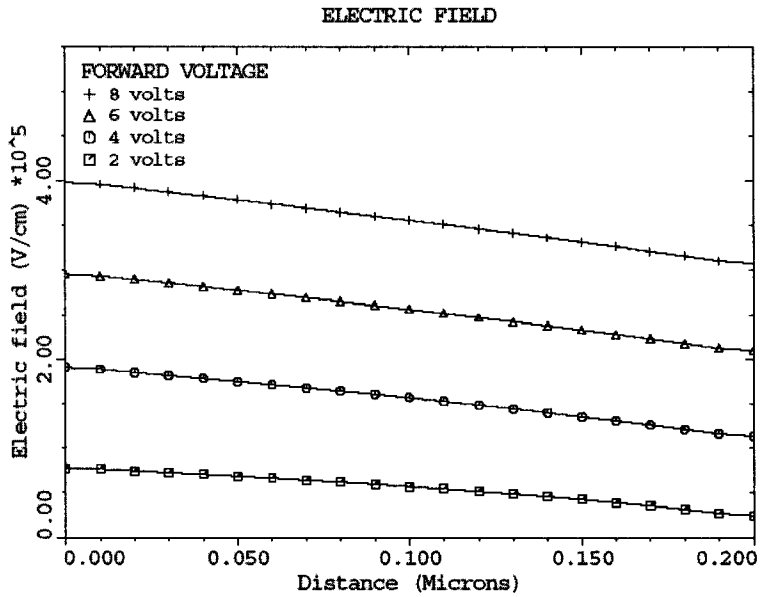

Figure 3-15 Electric field from cathode to anode with different forward bias.

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CHAPTER FOUR

ORGANIC FIELD EFFECT TRANSISTORS

4.1 Introduction

Pentacene is one of the most investigated organic materials for its reported high performance [75]. Pentacene-based devices such as Schottky diodes [76][77], thin film transistors (TFTs) [78][79][80], and integrated circuits [81] have been realized, and the electrical properties, as well as the magnetic properties [82] of pentacene, have been studied. Technology Computer-Aided Design (TCAD) based simulations [83][84] have also been performed to model the pentacene-based devices.

Of the parameters affecting the device performance, mobility is the key parameter of interest, which is a measure of the ease of charge transport in semiconducting materials. Currently, the highest reported mobility in pentacene appears to be 3 cm^2/Vs [85]. While the effects of temperature and electric field on mobility have been discussed in for pentacene [83][86], and for other organic materials in [87][88][89], much remains to be done to fully understand and characterize the mechanisms of charge transport in organic materials.

In this work, the temperature dependence of the hole mobility in pentacene has been studied over the range of 300 to 450 K. The effect of pentacene deposition rate on the hole mobility has also been investigated. Moreover, the electric field dependence

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of the hole mobility has been examined, and the field dependent mobility corrected for the effect of source and drain contact series resistance has been determined, and fitted by an empirical model. Based on the fabricated devices, two-dimensional modeling and simulation are carried out to identify significant parameters. The field dependent mobility model is developed for the fabricated devices.

4.2 Theory of Field Effect Transistors

A metal-insulator-semiconductor field-effect transistor (MISFET) is composed by a p-type (or n-type) semiconductor on which two electrode regions have been formed. Two ohmic contacts, the source and drain, are constructed on these two regions. The gate, which is used to modulate the conductivity of the source-drain channel, is isolated from the semiconductor substrate by an insulating layer. In the metal-semiconducting field-effect transistor (MESFET), the n-type (or p-type) source and drain are grown on an n-type (or p-type) substrate, and a Schottky barrier is used to isolate the gate electrode. Finally, the TFT consists of a thin semiconducting layer with two ohmic contacts and an isolated gate.

For the TFT, normally there are two kinds of structures under studies, Figure 4-1 [90], which are called top contact (TOC) (with source and drain electrodes located on the organic semiconducting layer) and bottom contact (BOC) (with the organic semiconductor located on the gate insulator and source/drain electrodes), separately.

The energy band diagram of an ideal MIS diode is given in Figure 4-2 for a p-type semiconductor. The diode is termed ideal because the bands are flat for zero applied voltage. This is the case when Equation 4-1 is satisfied.

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$$\phi_m - (\chi + \frac{E_g}{2q} + \phi_b) = 0 . \quad (4\text{-}1)$$

Here, ϕ_m is the metal workfunction, E_g is the semiconductor bandgap, q is the absolute electron charge, and ϕ_b is the potential difference between the Fermi level and the intrinsic Fermi level E_i.

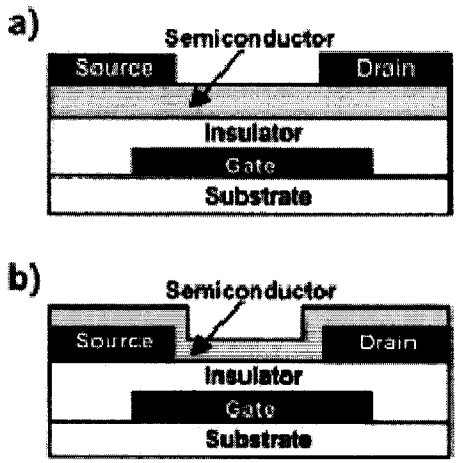

Figure 4-1 Organic FETs configuration: a) Top-contact; b) Bottom-contact [90].

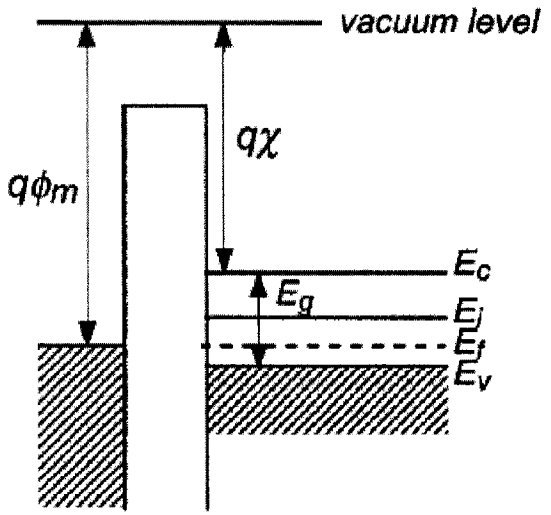

Figure 4-2 Band diagram of an ideal MIS structures at equilibrium.

When the MIS structure is biased with positive or negative voltages, three different situations may occur at the insulator/semiconductor interface. For a negative

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voltage, shown in Figure 4-3(a), the bands bend upward and the top of the valence band moves closer to the Fermi level, causing an accumulation of holes near the insulator-semiconductor interface. A depletion of majority carriers occurs in the case of a moderate positive voltage, as shown in Figure 4-3(b). When a larger positive voltage is applied to the metal, Figure 4-3(c), the bands bend even more downward and the intrinsic level eventually crosses the Fermi level. From this point of view, the density of electrons exceeds that of the holes, and one enters the inversion regime.

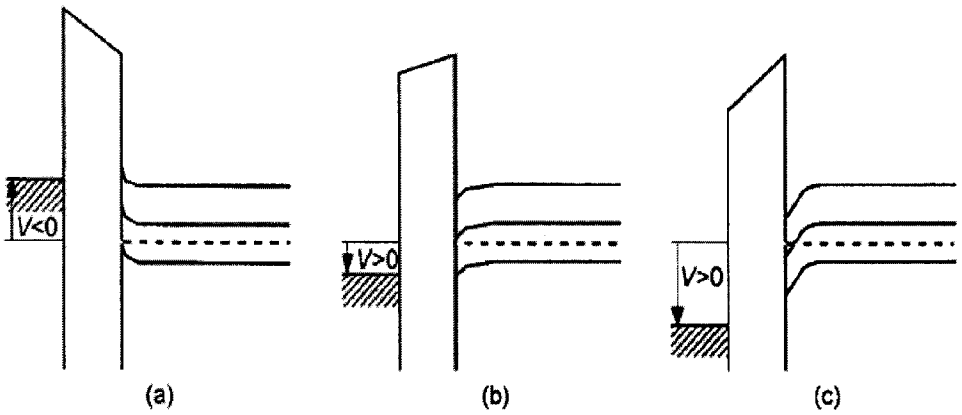

Figure 4-3 MIS structures under (a) accumulation, (b) depletion, and (c) inversion.

In all cases, the source contact will be assumed to be connected to the ground. When a sufficiently high positive voltage is applied to the gate of a MISFET, an inversion layer will form at the insulator-semiconductor interface, providing a conducting channel between the source and the drain. This turns the device on. One of the main advantages of the MISFET structure is that the depletion region between the p-type substrate and both the n-channel and the n regions below the source and drain contacts provides isolation from any other device fabricated on the same substrate. Very low off currents are also achieved because both n-type regions act as reverse-biased diodes. The current-voltage characteristics of the MISFET are calculated in the gradual channel (or

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Shockley) approximation [97] based on the assumption that the electric charge density related to a variation of the electric field along the channel is much smaller than that related to a variation across the channel, namely $|\partial F_x/\partial x| << |\partial F_y/\partial y|$, where F is the electric field, and x and y are the directions parallel and perpendicular to the insulator-semiconductor interface, respectively. This condition is generally fulfilled when the channel length L is much larger than the insulator thickness d_i. If we assume in addition that the charge mobility μ is constant, the drain current I_{ds} is related to the source-drain voltage V_{ds} and the source-gate voltage V_{gs} through Equation 4-2 [97],

$$I_{ds} = \frac{W}{L}\mu C_i\{(V_{gs} - 2\phi_b - \frac{V_{ds}}{2})V_{ds} - \frac{2}{3}\frac{\sqrt{2\varepsilon_s qN_a}}{C_i}[(V_{ds} + 2\phi_b)^{3/2} - (2\phi_b)^{3/2}]\} \quad (4\text{-}2)$$

Here, W is the channel width, C_i is the insulator capacitance (per unit area), ϵ_s is the semiconductor permittivity, and N_a is the doping level of the p-type substrate. Equation 4-2 predicts that the drain current first increases linearly with the drain voltage for a given gate voltage known as linear regime, then gradually levels off to a constant value known as saturation regime. It also predicts that the drain current increases when the gate voltage increases. For a small V_{ds}, Equation 4-2 reduces to Equation 4-3, where the threshold voltage V_{th} corresponds to the onset of the strong inversion regime, and is given by Equation 4-4,

$$I_{ds} = \frac{W}{L}\mu C_i(V_{gs} - V_{th})V_{ds} \quad (4\text{-}3)$$

$$V_{th} = V_{FB} + 2\phi_b + \frac{\sqrt{2\varepsilon_i qN_a(2\phi_b)}}{C_i} \quad (4\text{-}4)$$

where V_{FB} is the flat-band voltage.

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Two important technological parameters are the channel conductance g_{ds} and the transconductance g_m, which are represented by Equation 4-5 and Equation 4-6 in the linear regime, respectively. In the saturation regime, the drain current and transconductance are given by Equation 4-7 and Equation 4-8, respectively.

$$g_{ds} = \left|\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{Vgs=const} = \frac{W}{L}\mu C_i(V_{gs} - V_{th}) \tag{4-5}$$

$$g_m = \left|\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{Vds=const} = \frac{W}{L}\mu C_i V_{ds} \tag{4-6}$$

$$I_{ds,sat} = \frac{W}{2L}\mu C_i(V_{gs} - V_{th})^2 \tag{4-7}$$

$$g_m = \frac{W}{L}\mu C_i(V_{gs} - V_{th}) \tag{4-8}$$

The concept of the thin film transistor (TFT) was first introduced by Weimer in 1962 [91]. This structure is well adapted to low conductivity materials, and is now currently used in amorphous silicon transistors [92]. As seen in Figure 4-1, the source and drain electrodes form ohmic contacts directly to the conducting channel. Unlike both the structures described above, there is no depletion region to isolate the device from the substrate. Low off-state current is only guaranteed by the low conductivity of the semiconductor. A second crucial difference to the traditional MISFET is that, although the TFT is an insulated gate device, it operates in the accumulation regime and not in the inversion regime. For this reason, care has to be taken when transferring the equations of the drain current from the MISFET to the TFT. In fact, the absence of a depletion region leads to a simplification of Equation 4-2, which can now be written as Equation 4-9.

$$I_d = \frac{W}{L}\mu C_i(V_{gs} - V_{th} - \frac{V_{ds}}{2})V_{ds} \tag{4-9}$$

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Here, the threshold voltage is the gate voltage for which the channel conductance is equal to that of the whole semiconducting layer. It is given by Equation 4-10 [50], where N is the density of doping centers. Equation 4-10 assumes that all doping centers are ionized when the concentration of free carriers is much lower than that of trapped carriers, where N_t is the trap density:

$$V_{th} = \frac{\sqrt{2kT\varepsilon_r\varepsilon_0 N_t}}{C_i} \tag{4-10}$$

In the saturation regime, the current is given by Equation 4-7. It must be kept in mind that this equation was derived under assumptions that are not always fulfilled in organic semiconductors, particularly that of a constant mobility.

4.3 N-channel Field Effect Transistors

4.3.1 Introduction

Compared to the p-type organic materials, n-type organic materials have much lower mobility, and are more sensitive to the environments due to the transport mechanism for organic materials. Among several n-type materials, NTCDA is more promising due to its high mobility of 0.06 cm^2/Vs [93] and investigated stabilities [94].

In this section, the depletion-mode n-channel OFETs based on NTCDA are fabricated and characterized. From the discussions and analyses of charge transport and energy bands, the mechanism and function of this OFET are introduced and demonstrated. The mobility of 0.016 cm^2/Vs was obtained from $I_{ds} - V_{ds}$ data in the saturation region at $V_{gs} = 0$ V. The threshold voltage is -32 V (from $I_{ds} - V_{gs}$ data in the linear region by the linear extrapolation method ($V_{ds} = 20$ V)), the cut off current is 1.76 nA, and the on/off ratio at saturation region ($V_{ds} = 60$ V) is 2.25×10^2. The environmental effects

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(temperature, humidity, etc.) on the electrical properties of NTCDA will be under investigation. Further research to improve the properties of the OFETs may focus on the n-type organic semiconductors with higher carrier field-effect mobility, organic dielectrics with better quality, and conductive polymers with higher conductivity as the electrodes.

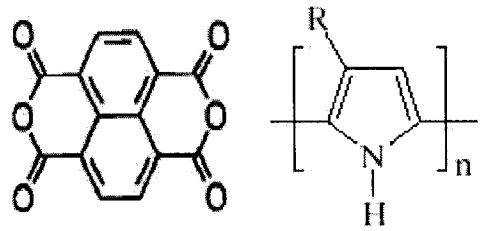

Figure 4-4 Molecular structures of NTCDA (left) and PPy (right).

4.3.2 Materials

In the fabricated transistors, NTCDA acts as the active channel material due to its n-type conduction [94]. P-type conductive polymer polypyrrole (PPy) is acted as the source and the drain in the transistors, showing good characteristics of the p-type conducting polymer [95]. Aluminum acts as the electrode for the source and the drain. Dielectric material is poly(4-vinylphenol) (PVP) dissolved in IPA (isopropyl alcohol). All the organic chemicals, undoped NTCDA powder, 20% wt PPy aqueous solution, and PVP solution, are purchased from Aldrich. Figure 4-4 shows the molecular structures of NTCDA and PPy.

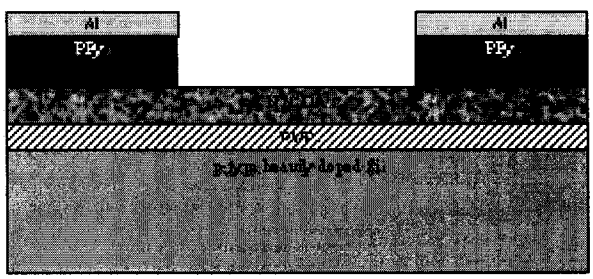

Figure 4-5 Structure of the n-channel FETs.

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4.3.3 Fabrication

Here, the top-contact (TOC) structure was employed in the devices, as illustrated in Figure 4-5. The width of the channel is 40 μm, and the length is 200 μm. As shown in the schematic figure, the devices are built on the heavily doped silicon wafer, which also acts as the gate electrode. First, a layer of PVP (800 nm thick) is spun on the wafer. Next, NTCDA 1.5 μm thick is thermally evaporated at the current of 20 amps and the working pressure of 1×10^{-7} Torr. After the evaporation of NTCDA, the PPy is deposited by the spin-coating technique, and 200 nm Al is thermally evaporated on top of the PPy. Lithography process is used to pattern Al, and reactive ion etching (RIE) process to form the source region and the drain region.

4.3.4 Results and Discussion

NTCDA-based OFETs were characterized in the atmosphere using the KEITHLEY TEST SYSTEM (236 Source Measure Unit). Figure 4-6 plots the output characteristics. Figure 4-7 and Figure 4-8 plot the transfer characteristics at V_{ds} = 20 V and V_{ds} = -60 V, respectively. In Figure 4-6, the drain current (I_{ds}) versus the drain voltage (V_{ds}) curve (output characteristics) shows the depletion-mode operation. With the decrease of the gate voltage, the drain current (I_{ds}) decreases correspondingly. The drain saturation current decreases quickly from V_{gs} = 0 V to V_{gs} = -20 V because the depletion occur at the PVP/NTCDA interface where most current is generated. With the further decrease of gate voltage, the region in the NTCDA channel away from the interface is depleted, which contribute less current. The drain current (I_{ds}) versus the gate voltage (V_{gs}), transfer characteristics, at linear output region (V_{ds} = 20 V) are shown in Figure 4-7, demonstrating the threshold voltage of -32 V by the linear extrapolation method and the

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cut off current of 1.76 nA. The on/off ratio can be extracted from the transfer characteristics at the saturation region (V_{ds} = 60 V) and is about 2.25 × 10^2, as shown in Figure 4-8. The electron mobility is calculated to be 0.016 cm^2/Vs from the models discussed in the former section, which is smaller than the results from the doped NTCDA [3] and larger than the former investigated undoped one [96].

The depletion-mode FETs are normally on due to the electric field built by the existed electrons in the channel region between the source and the drain with a certain voltage. For this type of device, it is functional even though the gate voltage (V_{gs}) is equal to zero. With the decrease of V_{gs} (V_{gs} is negative), the effective channel shrinks, and thus conduction ability of the active layer decreases simultaneously. Therefore, the drain current (I_{ds}) decreases until the active channel disappears and then the device is cut off. The gate voltage that turns off the device is known as turn-off voltage, which is also the threshold voltage where the active channel forms.

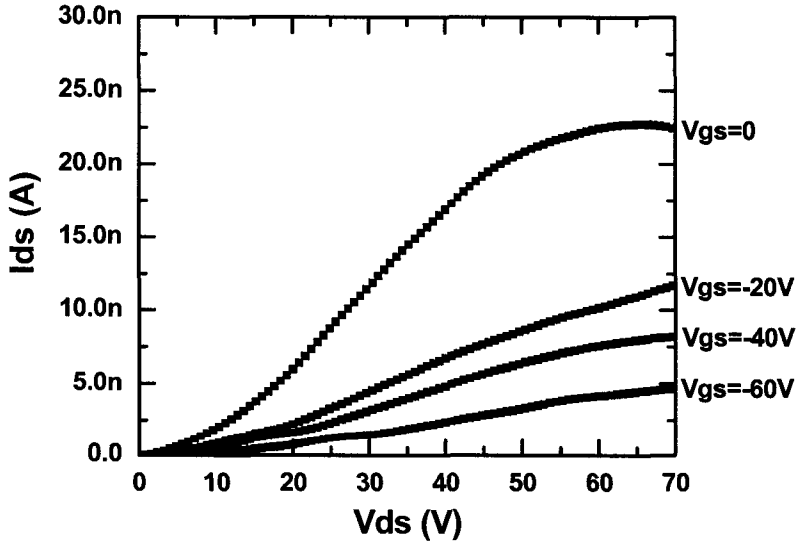

Figure 4-6 Output characteristics of the NTCDA FETs.

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Generally, the analytic models Equations 4-7 and 4-9 are employed to describe the behavior of organic transistors [97], transfer and output characteristics. They are rewritten here,

$$I_{ds} = \frac{WC_i}{L}\mu(V_{gs} - V_{th} - \frac{V_{ds}}{2})V_{ds} \qquad (Linear - region) \qquad (4\text{-}11)$$

$$I_{ds} = \frac{WC_i}{2L}\mu(V_{gs} - V_{th})^2 \qquad (Saturation - region) \qquad (4\text{-}12)$$

From the energy-band theory and the interfacial effect, the more insight of the OFET can be analyzed. Table 4-1 [98][99] gives the parameters (work function Φ, energy gap E_g, and Fermi level or effective Fermi level E_f) for the materials used in the fabricated OFETs. At the gate voltage of zero, the channel is completely open, and the electrons can be injected into the channel without barriers. The higher the drain current (V_{ds}), the more electrons injected. The largest drain current is obtained when the channel becomes saturation. When the gate voltage is decreased, the conduction band of heavily doped silicon will increase; thus, the positive charges are accumulated in the interface and negative charges are partly depleted in the channel. Moreover, the capability of electron-activated n-type channel is weakened. If the gate voltage is below the threshold voltage, the channel will be turned off, and the drain current will not be formed even collected with the high drain voltage.

Another issue is that the conducting channel is inside the bulk of the active layer for the depletion-mode operated devices compared to the channel at the interface between the dielectric layer and the active layer for the accumulation-mode operated devices, especially for the TOC structure.

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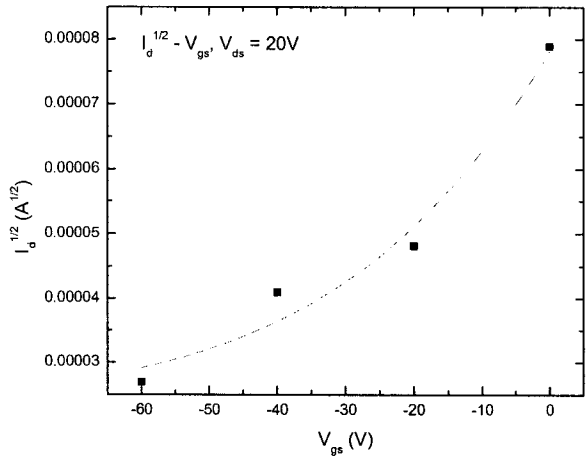

Figure 4-7 Transfer characteristics of the NTCDA FETs at V_{ds} = 20 V.

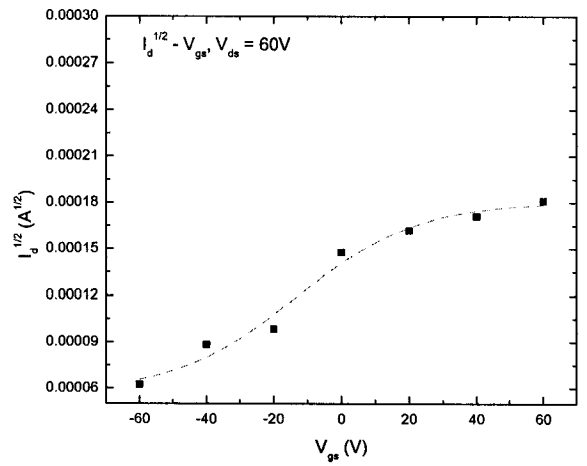

Figure 4-8 Transfer characteristics of the NTCDA FETs at V_{ds} = 60 V.

Table 4-1 Parameters of energy band for used materials in n-channel FETs.

Materials	Φ (eV)	E_g (eV)	E_C (LUMO) (eV)
NTCDA [98]	3.97	3.3	3.6
PPy [99]	5.19	3.16	2.5
P-type heavily doped Si	5.11	1.12	4.05

One of the most important applications of the depletion-mode OFETs is the load device of the inverter due to the symmetrical charging and discharging time constants,

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which is much faster than the inverter with the enhancement-mode transistors. Thus, the depletion-mode OFETs can be used in organic integrated circuits.

4.4 P-channel Field Effect Transistors

4.4.1 Fabrication

The schematic structure of the fabricated devices is shown in Figure 4-9. First, heavily-doped n-type silicon wafers were prepared and cleaned as a gate electrode as well as a substrate. Then, a 100 nm-thick layer of SiO_2 is grown on silicon by thermal oxidation and serving as the gate dielectric material. Subsequently, a layer of Au/Ti (80 nm/30 nm) is deposited by sputtering, followed by photolithography and wet etching to pattern the Au/Ti source and drain (S/D) contacts using the KI solutions and the BOE solutions. Pentacene (Aldrich, without purification) is then deposited on the channel (75 μm length and 1000 μm width) and S/D regions by thermal evaporation at 1×10^{-6} Torr through shadow mask. By holding the substrate at room temperature, a pentacene thin film (200 nm) is grown at two different deposition rates of about 4 Å/s and 8 Å/s, respectively.

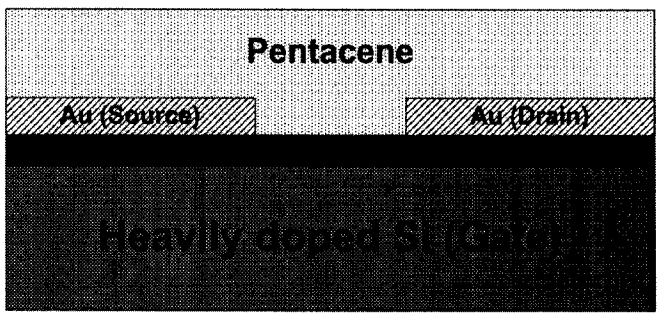

Figure 4-9 Schematic structure of fabricated pentacene TFTs.

The fabricated devices were tested with a Keithley Test System (236 source measure unit with H1001 heat control module) at atmospheric ambient condition. The output and transfer characteristics of the fabricated pentacene TFTs have been measured

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while sweeping the temperature from 300 to 450 K and then sweeping it back to observe annealing effects.

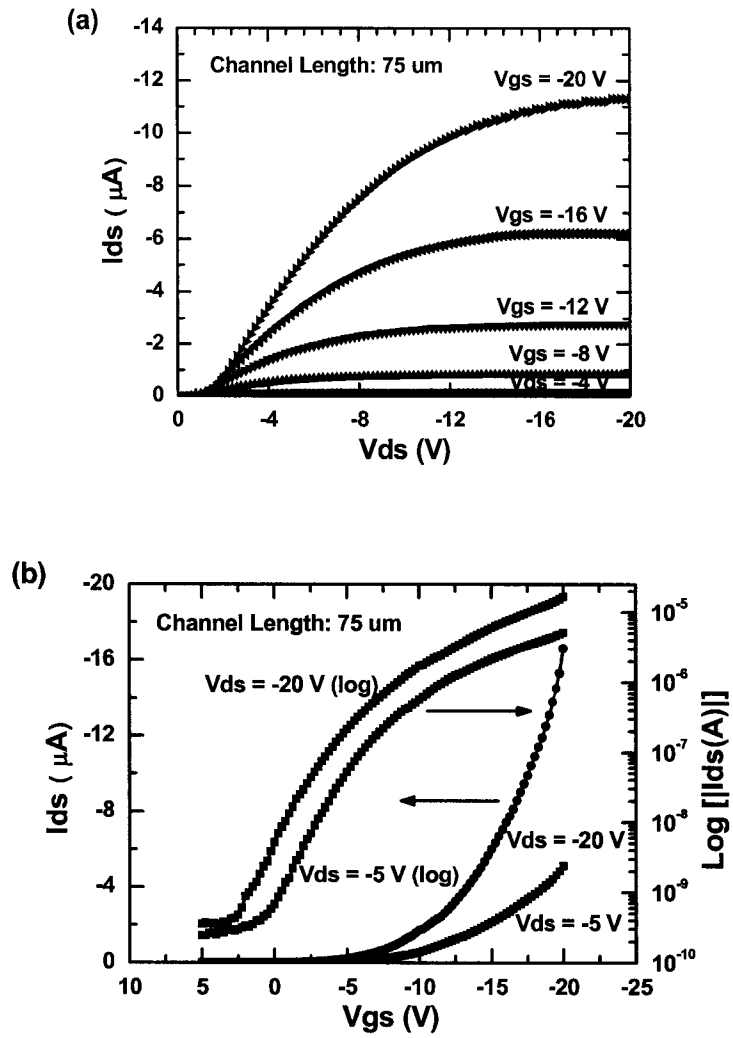

Figure 4-10 Output (a) and transfer characteristics (b) of pentacene TFTs.

4.4.2 Device Performance

The output and transfer characteristics of pentacene TFT, measured at room temperature, are shown in Figure 4-10 with a 75 μm channel length and a 1000 μm channel width, measured at room temperature. Pentacene has been thermally evaporated at 1×10^{-6} Torr and at a lower deposition rate (4 Å/s). These results are for the TFT at a

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lower deposition rate. Analogous results have also been measured for the TFT at a higher deposition rate, as shown in Figure 4-11 with a 25 μm channel length and an 800 μm channel width, measured at room temperature. Pentacene has been thermally evaporated at 1×10^{-6} Torr and at higher deposition rate (8 Å/s). The hole mobility calculated from Equations 4-11 and 4-12 gives the rough estimation compared to the traditional inorganic devices.

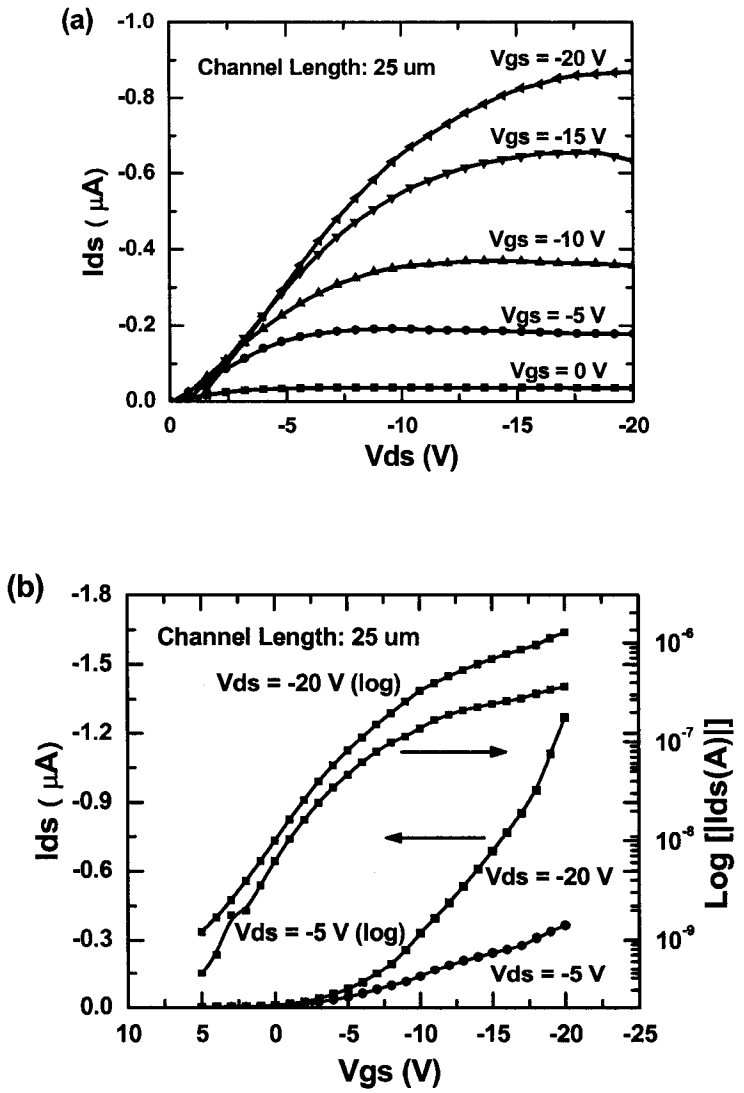

Figure 4-11 Output (a) and transfer characteristics (b) of pentacene TFTs.

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Based on the above equations and experimental data shown in Figure 4-10 and Figure 4-11, the device parameters for the pentacene TFTs at the lower deposition rate have been extracted, resulting in a saturation hole mobility of 0.26 cm^2/Vs from $I_{ds} - V_{gs}$ data in the saturation region at V_{gs} = -20 V by Equation 4-12 (lower mobility than [85] may result from non-purification, non-vacuum evaporation, etc.), a threshold voltage of -3.5 V from $I_{ds} - V_{gs}$ data in the saturation region by the linear extrapolation method (V_{ds} = -20 V), a subthreshold slope of 2.5 V/decade, and an on/off ratio of 10^5. For the pentacene TFTs at the higher deposition rate, hole mobility is 0.003 cm^2/Vs, a threshold voltage of 2.5 V, a subthreshold slope of 6 V/decade, and an on/off ratio of 10^3. The device performance from lower deposition rate is better than that from higher deposition rate. This may result from better growth quality of pentacene thin film. Since pentacene is the only active material in the TFTs, the performance is mostly determined by the charge transport in pentacene and the interfaces of pentacene/Au and pentacene/SiO_2. The ability of charge transport in pentacene is affected by processing conditions, including the deposition pressure and substrate conditions [90][100]. In the following section, it is shown that the hole mobility also appears to be related to the deposition rate.

4.4.3 Field Dependence

The electric field dependence of the hole mobility has also been examined in this study. When the drain voltage-generated lateral electric field is weak, the vertical electric field due to gate voltage can strongly influence the hole mobility. According to Equation 4-11 and its differential [101],

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{WC_i}{L}\mu V_{ds}, \qquad (4\text{-}13)$$

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where g_m is the transconductance. Using the above equation and experimental data, the field dependence of mobility can be determined. Figure 4-12 shows the field dependent hole mobility in pentacene TFTs at room temperature and V_{ds} = -5 V. The two sets of results presented are for TFTs fabricated at lower and higher deposition rates, respectively. In both cases, the mobility is noticeably increased by the increase in electric field at higher gate voltages, while, as observed earlier, the pentacene deposition rate also plays a major role in influencing mobility. The breakdown of the device occurs at a gate voltage of -90 V and a drain voltage of -105 V, which is high enough for a FET.

Unlike inorganic semiconductors, pentacene shows an increase in mobility with an increase in the gate voltage, as shown in Figure 4-12. This phenomenon is also reported in [88][102] for polycrystalline sexithiophene (6T). This gate-voltage dependent mobility is attributed to the trapping of charge carriers by the interfacial and bulk traps at lower values of the gate voltage [103]. As the gate voltage increases and more traps are filled, additional charge carriers move more freely through the channel, resulting in an increase in mobility.

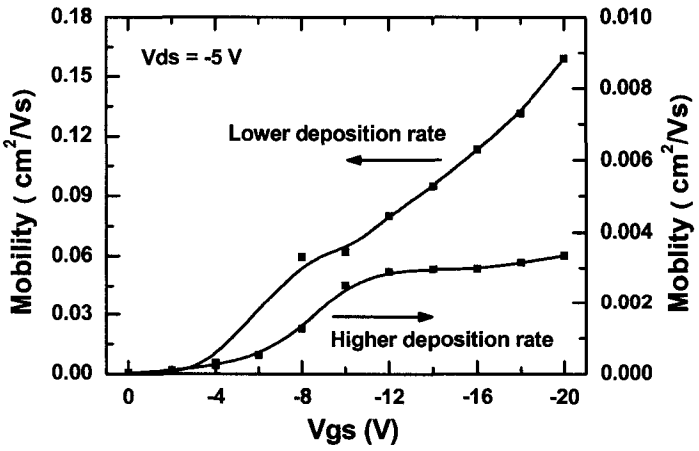

Figure 4-12 Gate voltage dependent mobility in pentacene TFTs at room temperature.

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4.5 Temperature Dependence of Mobility

Temperature and electric field dependence of the hole mobility in pentacene thin film transistors has been studied. Mobility is the key device parameter affecting performance in TFTs. The extracted plot of the hole mobility (from $I_{ds} - V_{gs}$ data in the linear or saturation region by Equations 4-11 and 4-12) as a function of temperature is shown in Figure 4-13 at V_{ds} = -20 V (saturation region) and V_{ds} = -5 V (linear region) for different gate voltages for pentacene TFTs at lower deposition rate (4 Å/s). It is found that over the temperature range of 300 to 450 K, the hole mobility increases to a peak value and then decreases to very low values. Previous experiments and analyses have indicated that thermally activated hopping transport occurs in some organic materials below room temperature [87][104]. Here, the hole mobility increases with temperature, displaying the Arrhenius behavior. But above room temperature, as the temperature is increased, the mobility in pentacene eventually decreases. This is attributed to the higher carrier scattering occurring at more elevated temperatures. Scattering phenomena increasingly dominate the behavior of transistors and thus determine the performance of the devices with the increase in temperature. Moreover, at higher temperatures, eventually pentacene ceases acting as an active material.

As illustrated in Figure 4-14, by fabricating the TFTs with higher pentacene deposition rate, a similar type of result and behavior is obtained at V_{ds} = -30 V (saturation region) and V_{ds} = -5 V (linear region) for different gate voltages for pentacene TFTs at a higher deposition rate (8 Å/s) as in Figure 4-13, except that there is over twenty times a reduction in the extracted hole mobility values. This is attributed to the change in the

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structure and morphology of the deposited pentacene layer, where higher deposition rate may result in less ordered layered structure of the pentacene film.

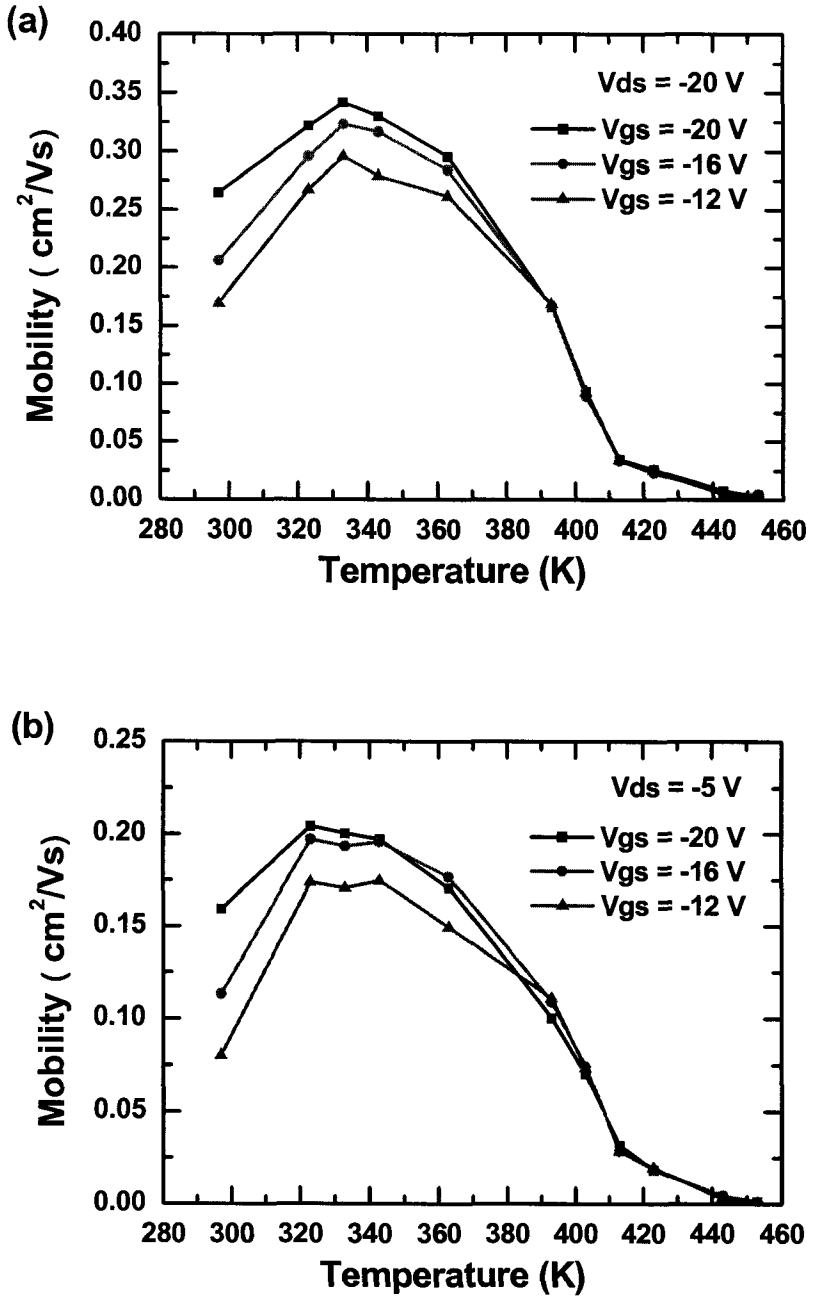

Figure 4-13 Temperature dependent mobility at V_{ds} = -20 V and V_{ds} = -5 V.

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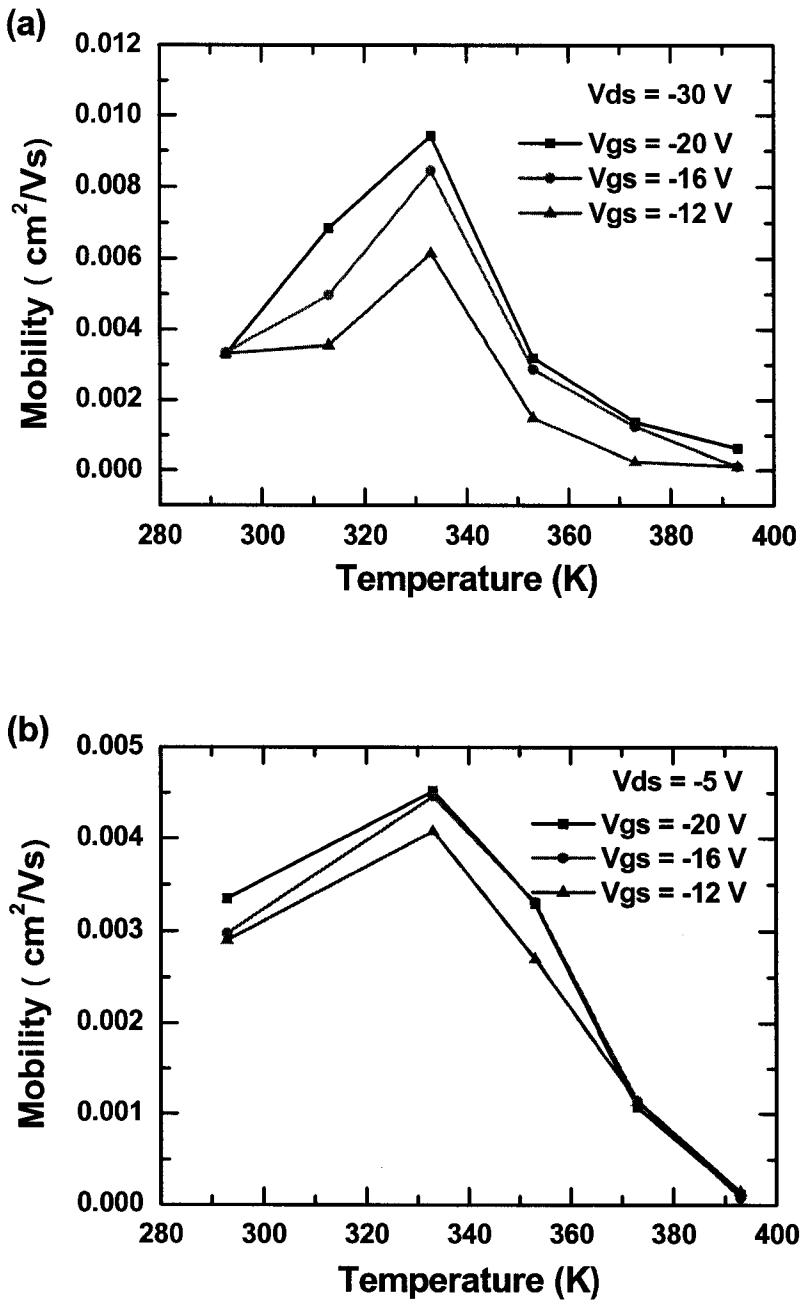

Figure 4-14 Temperature dependent mobility at V_{ds} = -30 V and V_{ds} = -5 V.

Besides mobility, several other important parameters have been extracted with temperature including threshold voltage (determined by the linear extrapolation method), subthreshold slope (at subthreshold region), off-state current (drain current observed at a

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gate voltage of 0 V and a drain voltage of -5 V), and drain saturation current (observed at both drain voltage and gate voltage of -20 V). The temperature dependencies of these parameters are quite similar to that of mobility.

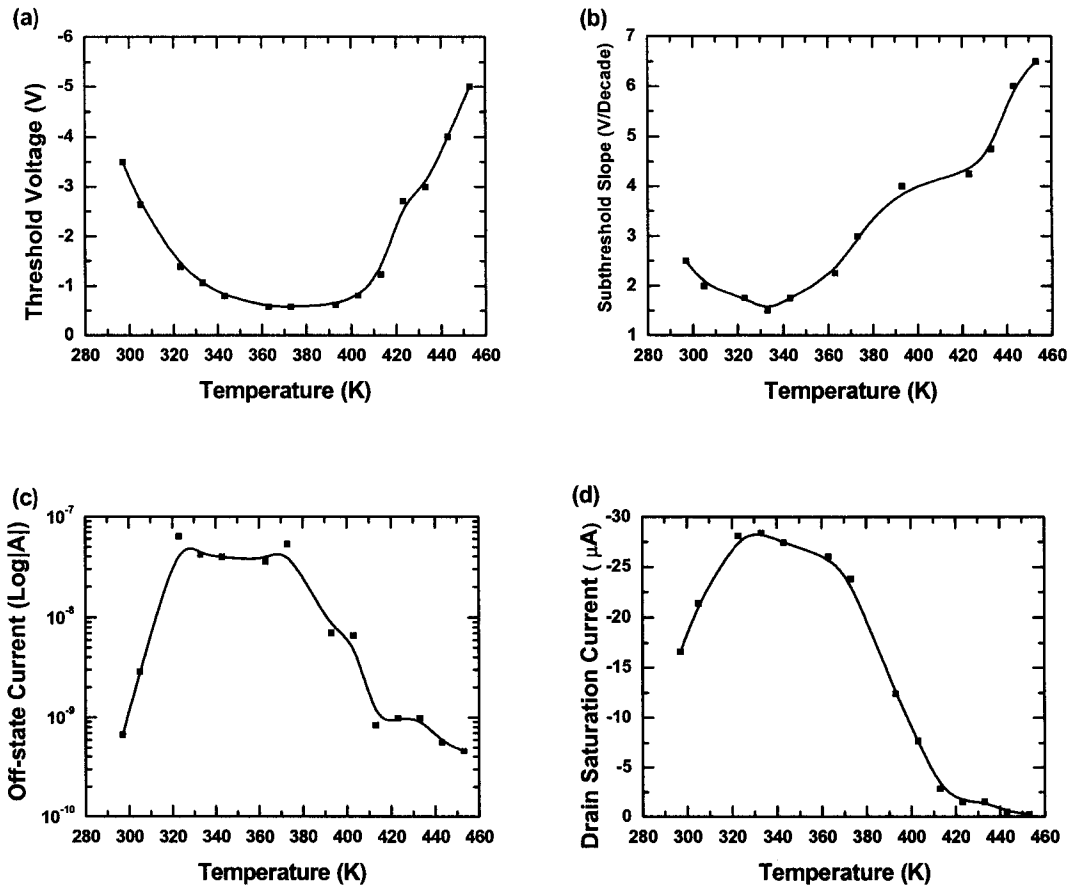

Figure 4-15 Temperature dependence of key parameters.

Figure 4-15 shows the temperature dependent (a) threshold voltage (V_{th}), (b) the subthreshold slope (S), the off-state current (I_{off}) at V_{gs} = 0 V and V_{ds} = -5 V, and (d) the drain saturation current (I_{dsat}) at V_{gs} = -20 V and V_{ds} = -20 V for different gate voltage in pentacene TFTs with a lower deposition rate, 4 Å/s. As demonstrated, the subthreshold slope, the off-state current and the drain saturation current all reach their peak around 330 K, except that the threshold voltage is around 370 K. For the TFTs considered, it has also

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been observed that by sweeping back the temperature and re-testing the devices again, almost the same device characteristics are measured up to a temperature of about 410 K, demonstrating no apparent thermal annealing effects below this temperature.

4.6 Modeling and Simulation

4.6.1 Introduction

With the development of organic microelectronics, Technology Computer-Aided Design (TCAD) based simulations are carried out to describe the behaviors of organic TFTs numerically based on different emphases: The effects of traps [105][106][107][108], field-dependent mobility models [83][109], device structures (bottom contact and top contact) [110], a variety of channel length [111], electrode contact [112], etc.

Since pentacene thin film are normally formed by deposition (such as evaporation) rather than grown as a single crystal, the thin film is of an amorphous or a polycrystalline nature with a great number of defects, which give rise to a continuous distribution of traps within the band gap [113]. The trap states exert strong effects on the electrical behavior of the device by trapping and holding carriers located within the channel. At the same time, interfacial charges are also introduced during the formation of pentacene thin film. Unlike the interface of Si/SiO_2 formed by thermal oxidation, the interface charges are significant due to the deposition process for organic/inorganic heterostructures. The interface charges contribute to the distribution of carriers near the interface of the channel/insulator, the most important region to field effect transistors. In the following parts of this section, we report a two-dimensional modeling and simulation of pentacene field effect transistors by the influence of bulk traps and interface charges.

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Moreover, a model for field dependent mobility will be applied to the fabricated device as demonstrated before. The TCAD tool Taurus-Device (Synopsys®) is employed to simulate the transfer characteristics and output characteristics of the fabricated devices.

4.6.2 Models

The simulated structure of the thin film transistor is shown in Figure 4-1. Two-dimensional simulations have been carried out using the standard drift-diffusion model implemented in the numerical program Taurus-Device [114]. The program solves the Poisson equation for the intrinsic potential,

$$\varepsilon\nabla^2\varphi = -q(p - n - N_A^- + N_D^+) - \rho_S \tag{4-14}$$

with the ionized acceptor and donor concentrations N_A^- and N_D^+, surface charge density ρ_S, electrostatic potential ϕ, and the continuity equations for the hole and electron densities p and n,

$$\frac{\partial n}{\partial t} = +\frac{1}{q}\bar{\nabla}\cdot J_n - U_n = F_n(\varphi, n, p) \tag{4-15}$$

$$\frac{\partial p}{\partial t} = \frac{-1}{q}\bar{\nabla}\cdot J_p - U_p = F_p(\varphi, n, p) \tag{4-16}$$

where U_n and U_p represent net electron and hole recombination, respectively. From Boltzmann transport theory, both the electron and hole current densities J_n and J_p and the charge carrier densities in the nondegenerate case are related to the quasi-Fermi potentials ϕ_{Fn} and ϕ_{Fp},

$$\vec{J}_n = -qn\mu_n\bar{\nabla}\varphi_{Fn} + qD_n\bar{\nabla}n = qn\mu_n\vec{E}_n + qD_n\bar{\nabla}n \tag{4-17}$$

$$\vec{J}_p = -qp\mu_p\bar{\nabla}\varphi_{Fp} - qD_p\bar{\nabla}p = qp\mu_p\vec{E}_p - qD_p\bar{\nabla}p \tag{4-18}$$

and

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$$n = n_i \exp\frac{\varphi - \varphi_{Fn}}{\phi_T} \tag{4-19}$$

$$p = n_i \exp\frac{\varphi_{Fp} - \varphi}{\phi_T} \tag{4-20}$$

with

$$n_i = \sqrt{N_C N_V} \exp\frac{-E_g}{2kT} \tag{4-21}$$

where ϕ_T is the thermal voltage, n_i is the intrinsic carrier concentration, N_C and N_V are the effective density of states for conduction band and valence band, and E_g is the band gap. Therefore, to simulate the electrical characteristics of the organic transistor, one has to specify the relevant material parameters. The relative dielectric constant is necessary for both the organic insulator and the organic semiconductor. In addition, the energy band gap E_g, the electron affinity χ, the effective densities of states N_C and N_V, the mobilities μ_n and μ_p and the doping concentration have to be defined for the active semiconductor pentacene. For example, for the effective densities of states [115], one has to use the molecular or monomer density of about 10^{20}-10^{21} cm^{-3}. In our simulations we use 1×10^{21} cm^{-3}, but there is no appreciable difference in the curves using the lower values 1×10^{20} cm^{-3}. The band gap and the electron affinity of pentacene are 1.8 and 3.2 eV, respectively [76]. For the mobility, the experimentally determined values are used, which are μ_p = 0.22 cm^2/Vs at V_{ds} = -20 V. The dielectric constant of pentacene is 3.0 [76]. With regard to the doping concentration, 10^{16}-10^{17} cm^{-3} can be estimated from [76]. We use 8×10^{16} cm^{-3} from our former experimental results for pentacene-based MIS capacitor. The gate, drain, and source electrodes made from gold are characterized in the simulations by the work function of 5.0 eV. A typical simulation input file is shown in Appendix B.

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In the following discussions, we will find the electrical characteristics of pentacene TFTs with a gate dependent mobility model. Furthermore, the influence of bulk traps and interfacial charges is investigated to fit both linear and saturation regions. A series of parametric studies are carried out regarding these issues. At last, sensitivity studies of mobility and doping concentration are carried out.

4.6.3 Gate Dependence of Mobility

Unlike traditional inorganic semiconductors, organic semiconductors normally show the increase of carrier mobility with the increase of electric field or gate voltage [83][109]. Here, we employ an empirical law to estimate the mobility [88],

$$\mu = \alpha(V_{gs} - V_{th})^{\beta} \tag{4-22}$$

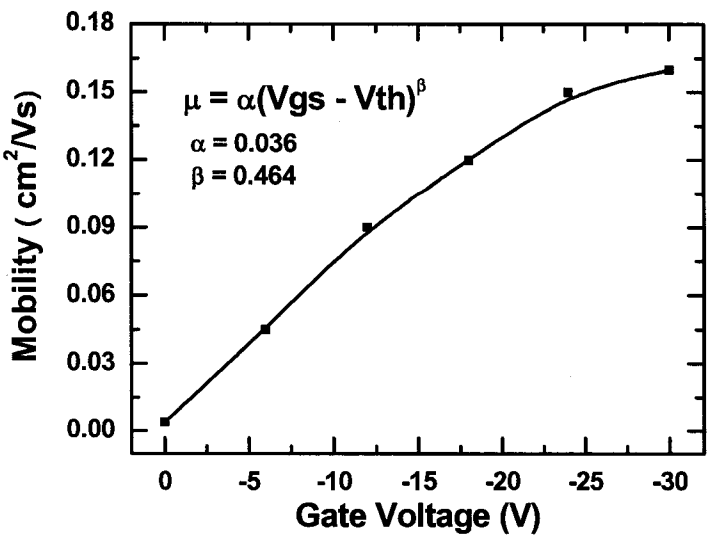

Figure 4-16 Gate voltage dependence of mobility in pentacene FETs.

Threshold voltage is calculated around -4.5 V using the linear extrapolation method from $I_{ds} - V_{gs}$ data at the saturation region. Figure 4-16 shows the relations of mobility and gate voltage for the fabricated device with $\alpha = 0.03625$ and $\beta = 0.46447$. By

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plugging in this model, output characteristics are simulated (dotted lines), as shown in Figure 4-17 with the comparison to experimental results (solid lines). We notice that the simulation results match well with experimental ones at linear regions for each gate voltage.

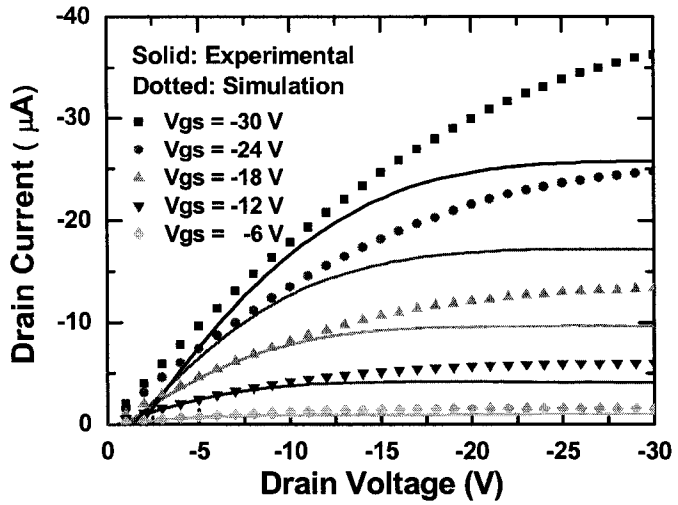

Figure 4-17 Simulation of output characteristics with gate dependence.

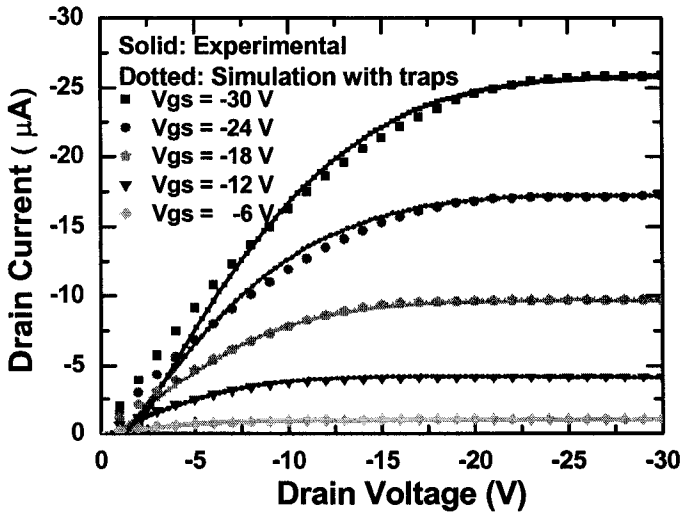

Figure 4-18 Simulation output characteristics of gate dependence and bulk traps.

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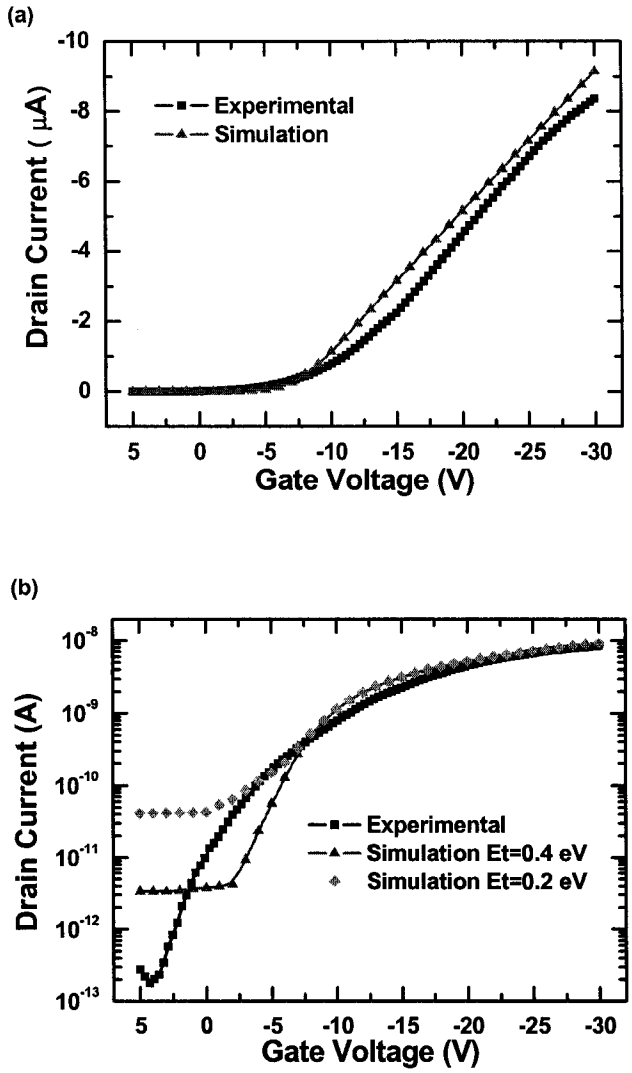

Figure 4-19 Simulation of transfer characteristics with bulk traps.

4.6.4 Influence of Traps

However, the discrepancy is quite large at the saturation region. This is attributed to the effect of reduced mobility of the transporting carriers. In organic semiconductors, this effect is mainly from the presence of bulk traps [50]. The trap levels can be filled by carriers induced by a gate voltage. By adjusting the amount of the density of bulk traps, the simulation results and experimental ones are matching well as shown in Figure 4-18, the saturation current (dotted lines) is pulled down with the gate-voltage dependent

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mobility and the presence of traps (7×10^{16} cm^{-3}) compared with experimental results (dotted lines). Discrepancies exist at the low drain voltage region, which may result from higher current in the fabricated device. Figure 4-19 shows the transfer characteristics with both simulation and experiments with linear scales in (a) and logarithm scales in (b). There exists little discrepancy, which is from the difference of I_{ds} from I_{ds}-V_{ds} and I_{ds}-V_{gs} characterization. A little memory effect exists during the measurement. We find that the trap level influences the subthreshold slope and off-state current, as shown in Figure 4-19(b), for trap level at 0.4 eV and 0.2 eV in comparison with experimental results. Obviously, lower the trap level (0.2 eV) provides better performances. The effect of traps to transfer characteristics is shown in Figure 4-20. Higher threshold voltage is obtained with more traps.

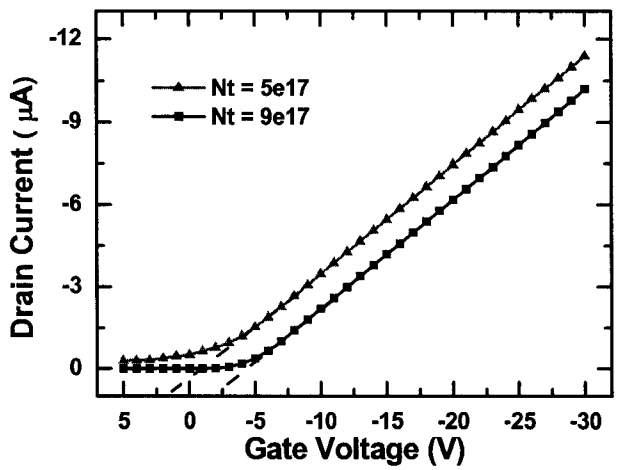

Figure 4-20 Influence of trap density to transfer characteristics of FETs.

Figure 4-21 shows the distribution of the electric field at different gate voltages when the device is working on the saturation region. We find that the electric field increases rapidly when closing to the semiconductor/insulator interface from the

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semiconductor part. At the bulk region of the channel which is far away from the interface, the electric field maintains a certain level corresponding to gate voltage applied. Similar phenomenon is found for the hole current, as shown in Figure 4-22 from channel to gate through the center of the channel. That demonstrates the importance of the semiconductor/insulator interface and indicates the large current formed from this region.

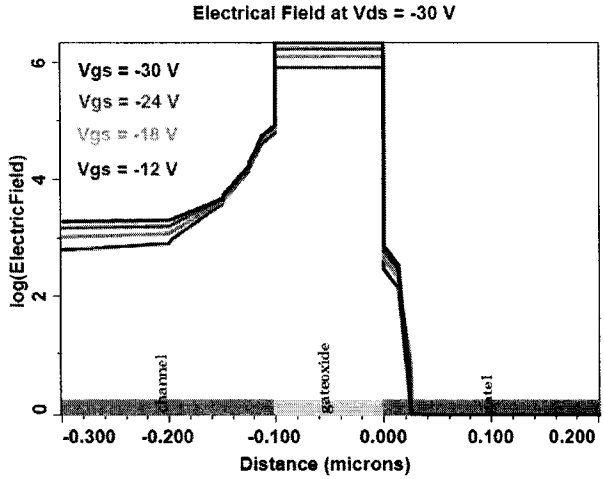

Figure 4-21 Distribution of electric field along the center of simulated FETs.

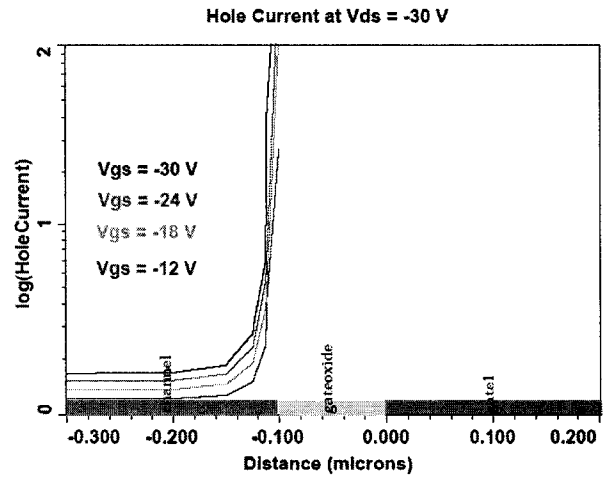

Figure 4-22 Distribution of hole current along the center of simulated FETs.

4.6.5 Studies of Sensitivity

Sensitivity studies are carried out for two parameters, mobility and doping concentration. As shown in Figure 4-23, transfer characteristics (V_{ds} = -5 V) and output

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characteristics (V_{gs} = -30 V) of FETs are at different mobility in the range of ±5%. We find that the changes of drain saturation current are ±5% correspondingly, which indicates the linear relations between drain saturation current and carrier mobility. The changes of off-state current are ±11%, and the changes of threshold voltage and subthreshold slope are quite small, around ±1%. These two parameters are insensitive to the change of mobility. A detailed of comparisons are shown in Table 4-2.

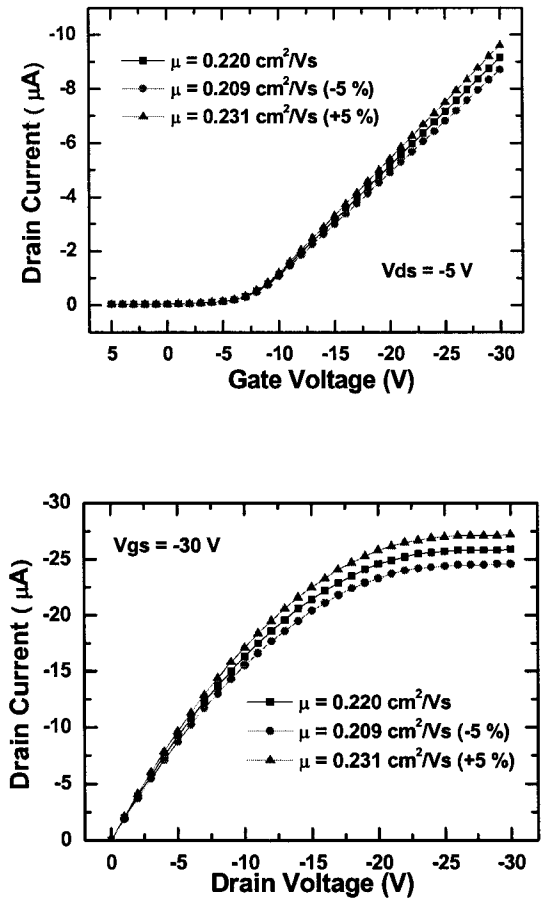

Figure 4-23 Transfer and output characteristics with change of hole mobility.

For doping concentration, we change it within ±5% in logarithmic scale. The simulation results for transfer and output characteristics are shown in Figure 4-24. We find that the device performance is dramatically influenced by doping concentration. For

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example, drain saturation current change is -18% and +50% with the change of doping concentration within ±5%, respectively. For off-state current, the change is over 100%. We identify doping concentration is a sensitive factor to the device performance. A detailed comparison is listed in Table 4-3.

Table 4-2 Sensitivity analysis of hole mobility.

Mobility (cm^2/Vs)	I_{dssat} (μA) ($V_{gs} = V_{ds}$ = -30 V)	I_{off} (pA) ($V_{gs} = 0$ and V_{ds} = -5 V)	V_{th} (V)	S (V/decade)
0.22	-25.9	-45	-7	~6
0.209 (-5%)	-24.6 (-5%)	-40 (-11%)	-6.9 (-1.4%)	~6
0.231 (+5%)	-27.2 (+5%)	-50 (-11%)	-7.1 (+1.4%)	~6

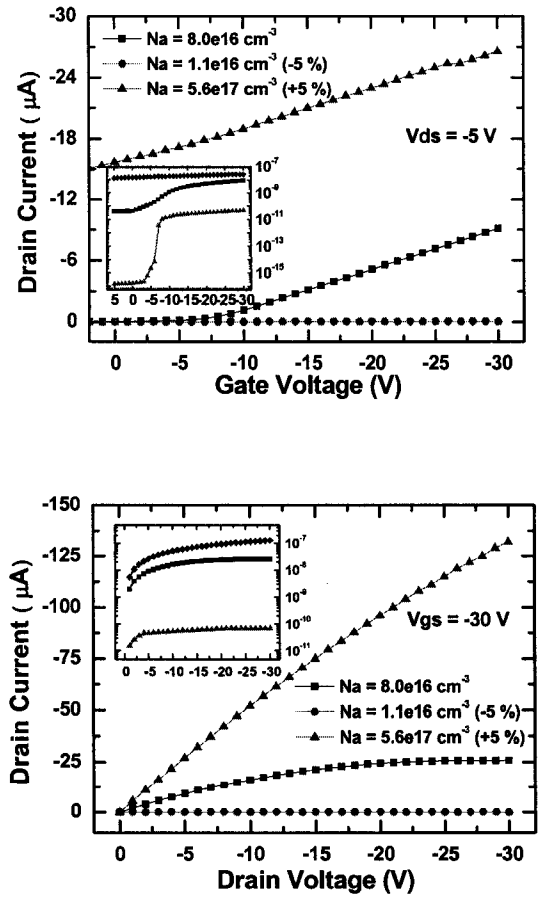

Figure 4-24 Transfer and output characteristics with change of doping concentration.

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Table 4-3 Sensitivity analysis of doping concentration.

Doping (cm^{-3})	I_{dssat} (μA) (V_{gs} = V_{ds} = -30 V)	I_{off} (pA) (V_{gs} = 0 and V_{ds} = -5 V)	V_{th} (V)	S (V/decade)
8.0×10^{16}	-25.9	-45	-7	~6
1.1×10^{15} (-5%)	-6.93×10^{-2} (-18%)	-1.6×10^{-4} (-330%)	-2.5 (-53%)	0.7 (-120%)
5.6×10^{17} (+5%)	-1.32×10^{2} (+50%)	-1.57×10^{4} (+154%)	>0	~12 (+39%)

4.7 Surface Modification

4.7.1 Introduction

Besides the effort of using advanced deposition methods [80] to improve the growth quality of pentacene thin film, different methods are employed to improve the condition at insulator/pentacene interface or source/drain contact and thus the profile of pentacene thin film. Pentacene is grown on a variety of substrates [75][116][117][118][119] and at different substrate temperatures [120][121][122]; buffer layers are used to modify the surface of the insulator [123][124]; or thermally grown SiO_2 surface is treated by oxygen plasma in [125]. Jackson, et al, used a self-organizing material octadecyltrichlorosilane (OTS) to form a well-ordered monolayer on thermally grown SiO_2 [45] while Kymissis, et al, modified the surface potential of contact by self assembled 1-hexadecanethiol monolayer [84]. Self assembled monolayer (SAM) has also been used in microelectronic devices [126][127].

Due to the importance of the insulator/semiconductor interface in Field Effect Transistors (FETs), it is necessary to investigate the relations between the interface properties and device characteristics for its dramatic influence to device performance. We propose an electrostatically assembled method to assist the surface modification at this interface. In our investigation, an assembled monolayer is grown before the deposition of pentacene. Both SiO_2/pentacene interface and source (or drain)/pentacene interface are

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modified by this process. The grown monolayer changed the property of the interface, and this change may affect the growth and morphology of pentacene subsequently. These changes contribute to significant improvements of the device performance.

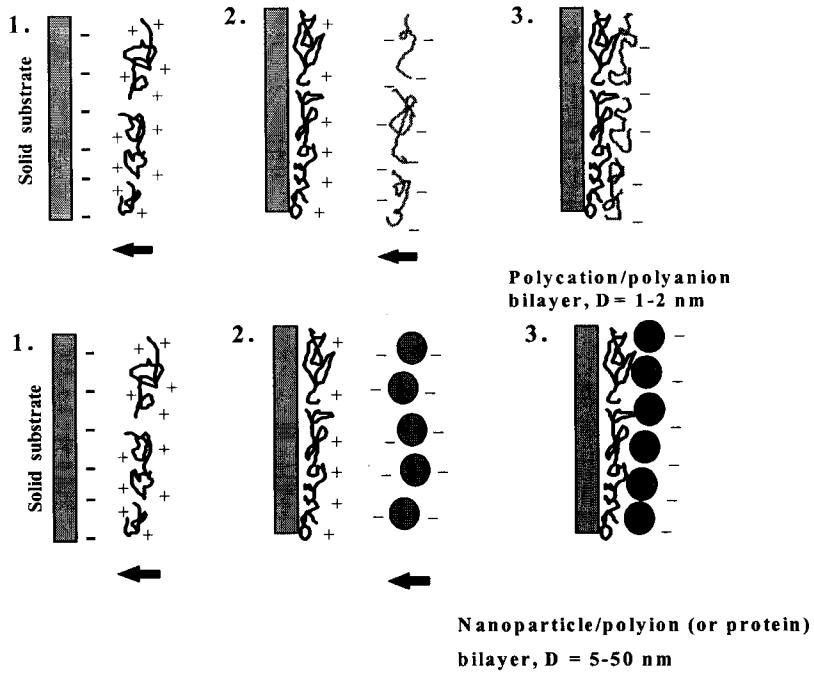

Figure 4-25 LBL assembly by alternate adsorption of polyions [135].

A technique for layer-by-layer (LBL) self-assembly of thin films by means of alternate adsorption of oppositely charged linear polyions was introduced in the early 1990s [128][129][130][131][132][133][134][135]. The basis of the method involves saturation of polyion adsorption, resulting in the reversal of the terminal surface charge of the film after the deposition of each layer. The method provides the possibility of designing ultra-thin multilayer films with a precision better than one nanometer of defined molecular composition as shown in Figure 4-25. The forces between nanoparticles and binder layers govern the spontaneous layer-by-layer self-assembly of ultrathin films. These forces are primarily electrostatic and covalent in nature, but they

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can also involve hydrogen bonding, hydrophobic and other types of interactions. The properties of the self-assembled multilayers depend on the choice of building blocks used and their rational organization and integration along the axis perpendicular to the substrate. Poly(dimethyldiallylammonium chloride) (PDDA) and poly(styrenesulfonate) (PSS) are positive and negative polyions, respectively, which are commonly used nanoparticles in self assembly technique as a precursor. By immersing the wafer in their solution alternatively, a thin self assembled film can be obtained. Normally, PDDA is grown firstly due to its good adhesion with substrates.

4.7.2 Experimental

A bottom-contact structure of the fabricated devices is schematically shown in Figure 4-9. Fabrication steps are similar except the presence of the assembled monolayer. First of all, heavily-doped n-type silicon wafers were prepared and cleaned as the gate electrode as well as the substrate. Second, 100 nm-thick layer of SiO_2 is grown on the silicon by thermal oxidation, and serving as the gate dielectric material. Subsequently, a layer of Au/Ti (80 nm/30 nm) is deposited by sputtering, followed by photolithography and wet etching to pattern the Au/Ti source and drain (S/D) contacts.

Samples are then separated into two groups. Group One labeled as "without assembled monolayer" is ready for pentacene evaporation. Samples in Group Two are then treated with sulfuric acid and hydrogen peroxide solution (3:7) at 70°C for 3 minutes. After that samples in Group Two are immersed in aqueous poly(dimethyldiallyl ammonium chloride) (PDDA, MW 200,000, Sigma) solution at a concentration of 15 mg/mL and pH 8 for 20 minutes. PDDA is the positively charged polyion, while SiO_2 surface is hydrophilic and shows negative charged after the treatment by the sulfuric acid

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and hydrogen peroxide solution. During the immersion, a monolayer of PDDA is self assembled through the electrostatic interaction and hydrogen bonding between PDDA nanoparticles and SiO_2 surface as well as good adhesion of PDDA to a free surface [136]. Actually, PDDA is one of commonly used materials to form precursor layers in layer-by-layer (LBL) self assembly technique [137][138][139][140]. When this monolayer is built up, electrostatic self assembly will stop accordingly. The thickness of the adsorbed PDDA monolayer is in precision of 1-2 nanometers and monitored by the Quartz Crystal Microbalance (QCM, USI-System, Japan) technique [141]. Then Group Two is labeled as "with assembled monolayer" and ready for pentacene evaporation. While the surface profile of the grown PDDA monolayer is not characterized, we have observed the surface profile after the deposition of pentacene by scanning electron microscopy (SEM).

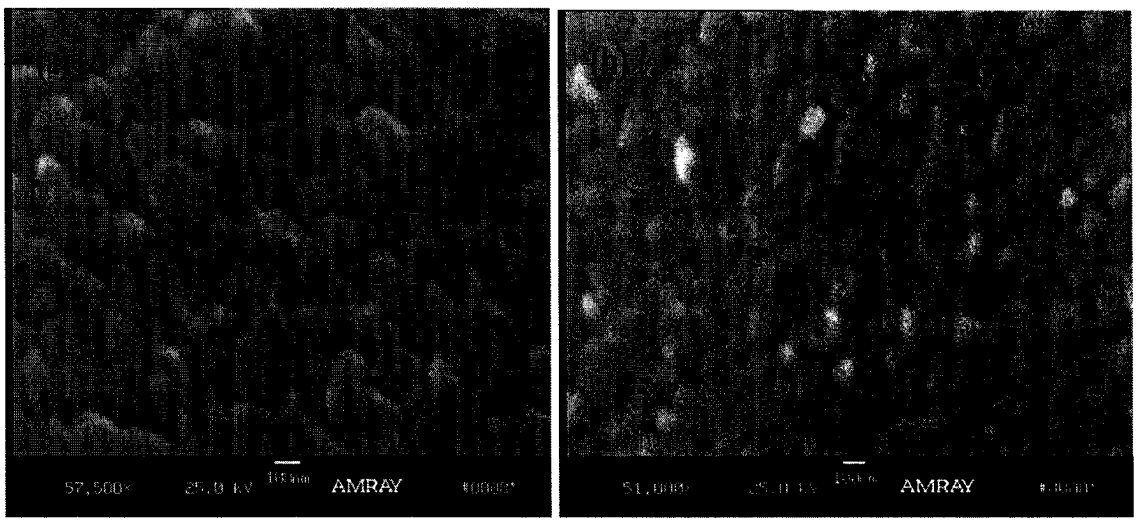

Figure 4-26 SEM for pentacene TFTs (a) without and (b) with assembled monolayer.

Pentacene (Aldrich, without purification) is then deposited on the channel (75 μm length and 1000 μm width) and source/drain regions by thermal evaporation at 1×10^{-6} Torr through shadow mask, for both groups at deposition rate about 6 Å/s. The thickness of pentacene thin film is 300 nm tested by a Tencor Surface Profiler. SEM observations

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of both groups are shown in Figure 4-26. The fabricated devices are tested by the Keithley Test System (236 source measure unit) at atmospheric ambient condition. The output and transfer characteristics of the fabricated pentacene TFTs have been measured for both samples with and without PDDA assembled monolayer.

4.7.3 Results and Discussion

Be adding a layer of assembled PDDA polyion in the channel/insulator interface, the performance of the device is improved significantly. The transfer characteristics I_{ds}-V_{gs} of devices with and without assembled monolayer are compared in Figure 4-27. Output characteristics of both devices are plotted in Figure 4-28. Equations 4-11 and 4-12 are employed to describe the behavior of organic transistors.

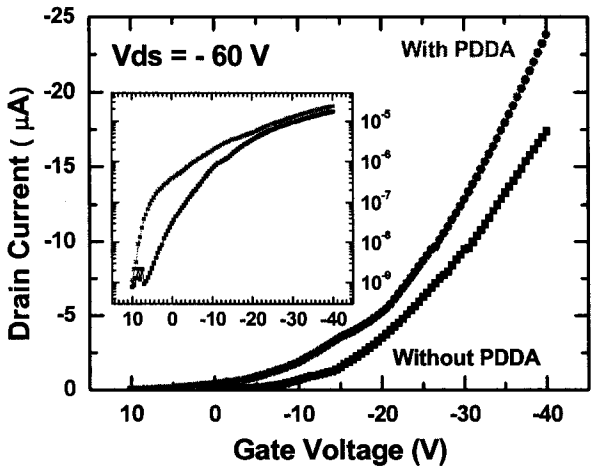

Figure 4-27 Transfer characteristics of TFTs without and with assembled monolayer.

Based on the above equations and experimental data, the device parameters for both groups of pentacene TFTs have been extracted and compared, as demonstrated in Table 4-4. The extracted parameters include threshold voltage (V_{th}) by the linear extrapolation method from $I_{ds} - V_{gs}$ data at saturation region (V_{ds} = -60 V), effective hole

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mobility (μ_{eff}), subthreshold slope (S), and on/off ratio, which are extracted from I_{ds}-V_{gs} at V_{ds} = -60 V (mobility is calculated by Equation 4-12 from I_{ds}-V_{gs} curves at V_{ds} = -60 V and V_{gs} = -40 V). From which, we find that the SiO_2/pentacene interface is successfully modified by assembled PDDA monolayer. Effective hole mobility μ_{eff} increases from 0.015 cm^2/Vs to 0.02 cm^2/Vs by 33%, the threshold voltage V_{th} decreases from -4.2 V to -2.45 V by -42%, the subthreshold slope S is largely improved from 4 V/decade to 2 V/decade by -50%, and the on/off ratio is slightly improved from 1×10^4 to 2×10^4 by 100%. At the same time, leakage current at low drain voltage is much decreased by the surface modification, which is extremely high for a device without assembled monolayer.

Insulator/organics interface plays an important role in organic thin film transistors [50], especially to subthreshold slope. Since PDDA is positively charged, it neutralizes the negative interfacial charges on the original SiO_2 surface (after the treatment of the BOE solution and the sulfuric acid and hydrogen peroxide solution [141][142][143]). Moreover, the assembled layer may reduce the physical defects and smooth the surface. Thus, most of the interface traps are expected to get reduced by this layer. The subthreshold slope affected by interface traps can be characterized by [144],

$$S = S_0 \frac{1+(C_S + C_{it})/C_i}{1+C_S/C_i} \tag{4-23}$$

and,

$$S_0 = \frac{kT}{q}\ln 10 \cdot (1+\frac{C_S}{C_i}) \tag{4-24}$$

where S_0 is the subthreshold slope without interface traps, C_S is the capacitance of accumulation layer in the organic semiconductor, C_i is the capacitance of insulator, and C_{it} is the capacitance associated with the interface traps which is in parallel with C_S. We

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assume here that the SiO_2/pentacene interface has no interface traps after the treatment of assembled monolayer. In the device with assembled monolayer, C_i should be substituted by the parallel of C_i and capacitance of assembled monolayer, C_{PDDA}. Since PDDA monolayer is very thin (1-2 nm compared to SiO_2 100 nm) and its dielectric constant is supposed to be very high (normally ten times higher for polyion films than thermally grown SiO_2 [137][145]), the parallel capacitance of C_i and C_{PDDA} is almost unchanged. Therefore, C_{it} can be calculated by Equations 4-23 and 4-24 and the density of the interface traps can be approximated by $C_{it} = eN_{it}$ [50]. A density of 7.0×10^{12} cm^{-2} is calculated for the device without assembled monolayer. Interface traps show similar negative influences to threshold voltage, effective hole mobility and on/off ratio in thin film transistors. By the modification of assembled monolayer, these parameters are improved. While it is believed that PDDA assembled monolayer also changes the surface energy of source/drain contact [84], it is not characterized quantitatively.

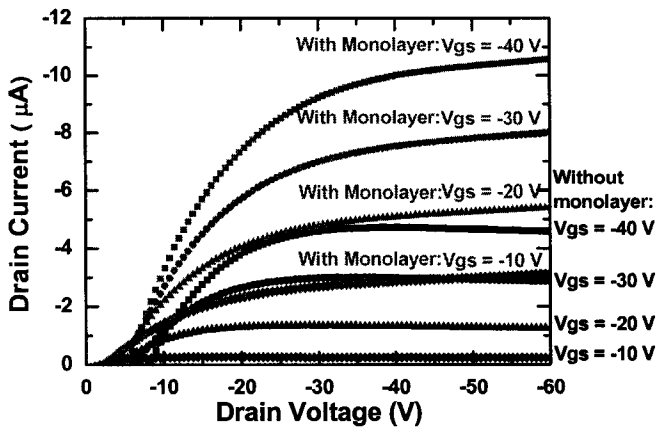

Figure 4-28 Output characteristics of TFTs without and with assembled monolayer.

The insertion of assembled monolayer may also affect the growth of pentacene resulting in different grain size. Surface profiles inspected by scanning electron

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microscopy (SEM) are shown in Figure 4-26. Surface profile without assembled monolayer shows irregular grain size with clear grain boundaries (Figure 4-26(a)), caused by an untreated surface. After the treatment of assembled monolayer, the surface condition are much improved and yield better surface profile of pentacene, as demonstrated in Figure 4-26(b), with smoother grain, more uniform grain size, and blurry grain boundaries though smaller.

The investigations and results presented here show that PDDA nano-scaled polyion can be used to modify the surface between insulator and active material in thin film transistors. By the immersion in the aqueous solution, PDDA nanoparticles form an ordered monolayer on SiO_2 through electrostatic self assembly. By the influence to the SiO_2/pentacene interface, the device performance is improved including higher effective mobility, lower threshold voltage, and lower subthreshold slope, etc.

Table 4-4 Comparison of pentacene TFTs without and with assembled monolayer.

	V_{th} (V)	μ_{eff} (cm^2/Vs)	S (V/decade)	on/off ratio
Without assembled monolayer	-4.20	0.015	4	10^4
With assembled monolayer	-2.45 (-42%)	0.020 (33%)	2 (-50%)	2×10^4 (100%)

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CHAPTER FIVE

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

In this project, organic microelectronic devices including capacitors, Schottky diodes, and field-effect transistors have been fabricated, characterized, and modeled. Main fabrication techniques used here include spin-coating, thermal evaporation, photo-lithography, electrostatic self assembly, and reactive ion etching. Numerical simulation tools, Taurus-Device and Medici (Synopsys®) are employed to model and simulate the fabricated devices.

From the capacitance-voltage (C-V) characteristics of the fabricated organic capacitors, consisting of insulating polymer poly(4-vinylphenol) (PVP), the dielectric constant of PVP is determined in both metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) structures, and the dielectric constant is found to be in the range of 5.6 – 5.94. The MIS structure is preferred over the MIM structure due to relatively simpler fabrication process steps and higher stability of the device characteristics. Pentacene is a commonly used organic semiconductor, whose hole density is determined to be about 8×10^{16} cm^{-3} from the MIS structure.

Based on the fabrication and characterization of Poly[2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene] MEH-PPV Schottky diodes, electrical characteristics

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including temperature-dependent mobility have been experimentally and theoretically investigated based on the current density-voltage (J-V) and capacitance-voltage (C-V) characteristics. To the best of our knowledge, this is the first investigation on the temperature dependence of mobility for MEH-PPV above the room temperature. As a part of this work, the space-charge limited conduction model and the field-dependent mobility model have been examined. They can describe the behavior of the fabricated Schottky diodes. The highest measured hole mobility of MEH-PPV is 0.013 cm^2/Vs at 353 K from the fabricated Schottky diodes. The effective carrier density of MEH-PPV is calculated to be 2.24×10^{17} cm^{-3}, which is useful for the simulation of the MEH-PPV based Schottky diodes. Several important factors, including barrier height and bulk traps are derived from simulations, which should be considered in the design of experiments and structures for Schottky diodes.

The organic field-effect transistors are investigated for n-type oligomer Naphthalene-tetracarboxylic-dianhydride (NTCDA). The NTCDA based transistors work on the depletion mode with a novel design consisting of organic dielectric, channel, and source/drain regions. The device characteristics have displayed the electron mobility of 0.016 cm^2/Vs, threshold voltage of -32 V, and on/off ratio of 2.25×10^2.

For field-effect transistors consisting of p-type organic semiconductor pentacene, the temperature dependence of mobility is studied experimentally, which also seems to be the first investigation for mobility above the room temperature. The deposition rate of pentacene affects the performance of the field-effect transistors. At room temperature, the device characteristics have displayed the hole mobility of 0.26 cm^2/Vs, threshold voltage of -3.5 V, subthreshold slope of 2.5 V/decade, and on/off ratio of 10^5 for the lower

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deposition rate of pentacene, and the hole mobility is 0.003 cm^2/Vs, threshold voltage of 2.5 V, subthreshold slope of 6 V/decade, and on/off ratio of 10^3 for the higher deposition rate of pentacene. The transistors with the lower deposition rate of pentacene offer better device performance. This demonstrates the importance of process control. Numerical simulations identify the effect of field dependence of mobility and the influence of bulk traps, which are crucial to the operation of organic field-effect transistors.

At last, the insulator/semiconductor interface is modified by electrostatically assembled monolayer (Poly(dimethyldiallylammonium chloride) (PDDA)). With the treatment of this assembled monolayer, the performance of pentacene FETs is improved significantly including higher effective hole mobility by 33%, lower threshold voltage by -42%, and lower subthreshold slope by -50%. This appears to be the first application of electrostatically assembled monolayer in field-effect transistors to our knowledge. This technique can be extended to other devices such as capacitors and diodes for the performance improvement.

5.2 Future Work

The field of organic electronics is still under development. Though conducting polymer/oligomer has disadvantages, such as high resistivity and low carrier mobility, these parameters have been much improved during the last three decades. The performance of organic electronic devices and circuits will be further improved continually with the studies in material properties, device structures, and fabrication techniques.

Several works can be considered for the extension of this project in the future. For organic capacitors, electrostatically assembled monolayer can be introduced to

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organic/metal or insulator/organic interface to improve the device performance. Furthermore, new and better materials can take the place of PVP as an insulator and pentacene as an active layer. The frequency dependence of capacitance of organic capacitors can be investigated. Further simulations can be carried out based on better understanding of the conduction mechanism of organics.

For Schottky diodes, an electrostatically assembled monolayer can be introduced to organic/metal or insulator/organic interface of MEH-PPV Schottky diodes for improvement. The space-charge limited conduction model and field-dependent mobility model can be developed and applied in numerical simulation, which will benefit the studies of conduction mechanism in organic materials. New models can be generated with the aid of simulation and modeling. Furthermore, light-emitting diodes and solar cells can be developed based on the fabricated Schottky diodes. More than one layer of organics can be involved in the light-emitting diodes and solar cells to improve the performance of devices.

Since the reactive ion etching technique is employed in the experiments, the degradation of organics may be introduced by this process. By etching organics other than oxygen in reactive ion etching, the degradation can be estimated or determined.

For field-effect transistors, fabrication techniques like the ink-jet printing and novel device structures such the dual-gate and three dimensional structures can be proposed to improve the device performance. The investigation on temperature dependence of mobility can be extended to a wider range. Numerical simulation can be employed for device performance optimization. Experiments can be performed to verify the optimal design.

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The experiments can be proposed to characterize the properties of the electrostatically assembled monolayer. Electrostatically assembled monolayer can be further studied to yield better improvements. Other nanoparticles, like poly(styrenesulfonate) (PSS), and more layers of assembled nanoparticles can be tested for their effects on the device performance.

Furthermore, organic light-emitting diodes and organic field-effect transistors can be combined together to realize organic active-matrix displays. All of these investigations may contribute and benefit the development of organic electronics.

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APPENDIX A

SIMULATION MODULE FOR ORGANIC SCHOTTKY DIODES

```
$ Simulation: Medici

MESH    ^DIAG.FLI
X.MESH  X.MAX=10  H1=1.0
Y.MESH  Y.MAX=0.2 H1=0.01

REGION  NAME=ACTIVE  SILICON
ELECTR  NAME=CATHODE TOP
ELECTR  NAME=ANODE   BOTTOM x.max=1.0

PROFILE  P-TYPE N.PEAK=3E17 UNIF
TRAPS    E1=-0.4 MIDGAP TAUN="1E-5" TAUP="1E-6" N.TOT="-3E17"
REGRID   DOPING LOG RAT=3 SMOOTH=1

CONTACT  NAME=CATHODE RESIST=1.375E6 WORKFUNC=4.3
CONTACT  NAME=ANODE   RESIST=1.375E6 WORKFUNC=4.7
MATERIAL SILICON PERMITTI=3 AFFINITY=2.8 EG300=2.2
```


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```
MATERIAL SILICON NC300=1E21 NV300=1E21

MOBILITY SILICON MUP0=0.00006


MODELS   SRH AUGER

SYMB     NEWTON CARRIERS=1 HOLE

LOG      OUT.FILE=iv_50.ivl

SOLVE    V(CATHODE)=0.0

SOLVE    V(ANODE)=-5.0 ELEC=ANODE VSTEP=0.1 NSTEP=100


SAVE     OUT.FILE=s1-50


$ END OF INPUT.
```

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APPENDIX B

SIMULATION MODULE FOR ORGANIC FETS

```
#Simulation: Taurus-Device


Taurus{device}


#Device Definition
DefineDevice( Name=tft, minx=0, maxx=95,  miny=-0.3, maxy=0.5,
   region(material="silicon", name="channel"),
   region(material="oxide", name="gateoxide"),
   region(material="silicon", name="gate1"),
   regrid(GridProgram="NonLevelSet", mindelta=0.02, maxdelta=0.4) )


#Device Regions
DefineBoundary(region="channel", polygon2d(point(x=0.0, y=-0.3),
   point(x=95um, y=-0.3), point(x=95um, y=-0.1um), point(x=0.0 ,   y=-0.1um ) ) )
DefineBoundary(region=gateoxide, polygon2d(point(x=0.0, y=-0.10um),
   point(x=95um, y=-0.10um), point(x=95um, y=0.0um), point(x=0.0, y=0.0um) ) )
DefineBoundary(region=gate1, polygon2d(point(x=0.0, y=0.0um),
   point(x=95um, y=0.0um), point(x=95um, y=0.5um), point(x=0.0, y=0.5um) ) )
Regrid(GridProgram="NonLevelSet", minDelta=0.02um, maxDelta=0.4um)
```


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```
Regrid(GridProgram="NonLevelSet", minDelta=0.01um, maxDelta=0.2um)
Regrid(GridProgram="NonLevelSet", minDelta=0.02um, maxDelta=0.2um,
  minY=0.0,maxY=0.1um, minX=7.5um, maxX=12.5um)
Regrid(GridProgram="NonLevelSet", minDelta=0.02um, maxDelta=0.2um,
  minY=0.0um,maxY=0.1um, minX=82.5um, maxX=87.5um)

#Flat Contacts
DefineContact(name=source, X(min=0.0, max=10um), Y(min=-0.21, max=-0.1um) )
DefineContact(name=drain, X(min=85um, max=95um), Y(min=-0.21um, max=-0.1um) )
DefineContact(name=gate, X(min=0.0, max=95um), Y(min=0.5um, max=0.5um) )
Contact(name=drain, workfunction=5.0)
Contact(name=source, workfunction=5.0)
Contact(name=gate, workfunction=4.1)

#Doping
Profile(name=Ptype, uniform(value=8e16), region=channel)
Profile(name=Ntype, uniform(value=2e20), region=gate1)

setBias(value= 0.0) {Contact(name=drain, type=contactVoltage){tft} }
setBias(value= 0.0) {Contact(name=source, type=contactVoltage){tft} }
setBias(value= 0.0) {Contact(name=gate, type=contactVoltage){tft} }

setAttributes{Traps(material=silicon, region=channel,
```

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```
trap(ilevel=0, dgen=2, et=-0.4, nt=-1e16, taup=1e-5) ) }

Physics(silicon(HoleContinuity(Mobility (Constant=true, mup0=0.045)))
Physics(Global(Global(ConductionDensityOfStates (AtRoomTemperature=1e21),
   ValenceDensityOfStates (AtRoomTemperature=1e21), Bandgap (Eg300=1.8) ) ) )
Physics(Silicon(Global(Permittivity=3, ElectronAffinity=3.2, WorkFunction=4.6) ) )

# Specify zero-carrier solution
Solve{couple(iterations=50, LinearSolver=direct){Poissons} }

# Specify one-carrier solution with electrons
Symbolic (carriers=2)

# Solve Output Characteristics
Solve{Ramp(RampSpecification( endValue=-6, nsteps=6)
   {BiasObject(name=gate, type=ContactVoltage){tft} } )
   {couple( iterations=20, LinearSolver=direct)
   {Poissons, ElectronContinuity, HoleContinuity} } }
solve{ramp(rampSpecification(endValue=-31, nsteps=31)
   {BiasObject(type=contactVoltage, name=drain) } ) }

# End of program.
```

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