Winter 2006

Nanodot-based organic memory devices

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NANODOT-BASED ORGANIC MEMORY DEVICES

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree of
Doctor of Philosophy in Engineering

COLLEGE OF ENGINEERING AND SCIENCE
LOUISIANA TECH UNIVERSITY

February 2006

LOUISIANA TECH UNIVERSITY

THE GRADUATE SCHOOL

11/14/2005
Date

We hereby recommend that the dissertation prepared under our supervision by Zhengchun Liu

entitled Nanodot-Based Organic Memory Devices

be accepted in partial fulfillment of the requirements for the Degree of Doctor of Philosophy in Engineering

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ABSTRACT

In this study, resistor-type, diode-type, and transistor-type organic memory devices were investigated, aiming at the low-cost plastic integrated circuit applications. A series of solution-processing techniques including spin-coating, inkjet printing, and self-assembly were employed to fabricate these devices.

The organic resistive memory device is based on a novel molecular complex film composed of tetracyanoquinodimethane (TCNQ) and a soluble methanofullerene derivative [6,6]-phenyl C61-butyric acid methyl ester (PCBM). It has an Al/molecules/Al sandwich structure. The molecular layer was formed by spin-coating technique instead of expensive vacuum deposition method. The current-voltage characteristics show that the device switches from the initial 'low' conduction state to 'high' conduction state upon application of external electric field at room temperature and return to 'low' conduction state when a high current pulse is applied. The on/off ratio is over 10^6. Each state has been found to remain stable for more than five months, even after the external electric field is removed. The PCBM nanodots wrapped by TCNQ molecules can form potential wells for charge trapping, and are believed to be responsible for the memory effects.

A rewritable diode memory device was achieved in an improved configuration, i.e., ITO-PEDOT:PSS-PCBM/TCNQ-Al, where a semiconductor polymer PEDOT:PSS is used to form p^+-N heterojunction with PCBM/TCNQ. It exhibits a diode characteristic (low conductive) before switching to a high-conductive Poole-Frenkel regime upon

applying a positive external bias to ITO. The on/off ratio at +1.0 V is up to 10^5. Simulation results from Taurus-Medici are in qualitative agreement with the experimental results and the proposed charge storage model.

The transistor-type memory device is fabricated on a heavily doped n-type silicon (n^+-Si) substrate with a 100 nm thick thermally-grown oxide layer. The n^+-Si serves as the gate electrode, while the oxide layer functions as the control gate dielectric. Gold nanoparticles as the charge storage units are deposited on the substrate by electrostatic self-assembly method. A self-assembled multilayer of polyelectrolytes, together with a thin spin-coated poly(4-vinyl phenol) layer, covers the gold nanoparticles and separates them from the poly(3-hexyl thiophene) channel. Conducting polymer PEDOT:PSS is inkjet printed to form the source/drain electrodes. The device exhibits significant hysteresis behavior in its I_{ds}-V_{gs} characteristics. The charge storage in gold nanodots (diameter =16 nm) was confirmed by comparing with devices having no gold nanoparticles, although the effects of interfacial traps may be also significant. The data retention time of the transistor memory is about 60 seconds, which needs to be further improved. It appears that this is the first demonstration of memory effects in an organic transistor caused by charge storage in metal nanodots in the gate dielectric. Therefore, the approach reported in this work offers a new direction to make low-cost organic transistor memories.

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ACKNOWLEDGMENTS

There are only two ways to live your life. One is as though nothing is a miracle. The other is as though everything is a miracle.

----Albert Einstein

It is usually the small things that determine the directions of our lives. Since I stepped in the door of the Institute for Micromanufacturing (IfM) at Louisiana Tech University, my life has always been influenced by those 'small things'—materials and devices at the scale of micrometer or even nanometer. As a matter of fact, they have become one of the most important parts of my life now. And, yes, they are miracles!

In the past four years, I delighted in such a wonderful world of devices, molecules, and electrons. Therefore, I would like to express my deepest gratitude and appreciation to my advisory committee chair Dr. Yi Su and co-chair Dr. Kody Varahramyan. It is them who led me to the field of organic electronics. Their guidance and encouragement have been critical to my exploration in this mysterious part of the great nature. They are also my learning models of the scientific spirit and positive attitude.

I am also very grateful to Dr. Yuri Lvov, Dr. Chester Wilson, and Dr. Alfred Gunasekaran for their precious advice and serving as the advisory committee members.

Special acknowledgements extend to the staff at IfM. I thank Mr. Dee Tantaum, Mr. John McDonald, Dr. Karen Xu, Mr. Ji Fang, Ms. Debora Wood, and Mr. Scott

Williams for their support and help with the experiments. I thank Abdul Khaliq for his valuable help with the simulation part of this work.

Much gratitude also goes to my group mates Mr. Fengliang Xue, Mr. Rajneek K. Khilan, Ms. Jie Liu, Mr. Rohit Dikshit, and Mr. Razat Nohria for their helpful discussion, support and contributions. There are many other people who influenced my work and assisted for my progress: Dr. Zonghuan Lu, Dr. Difei Qi, Mr. Chuanding Cheng, Ms. Ling Zhang, Ms. Qiushu Zhang, Dr. Xiaodong Yan, Dr. Weisong Wang, Mr. Qi Chen, and Mr. Aravind Chamati. I thank them for their help with the experiments and for the discussions.

I want to present my special thanks to my parents and my brother for their love, support and encouragement accompanying me through both sunny days and rainy days.

Last but surely not least, deep in my heart, I want to thank my wife Yingxu Kuang for her love and taking care of everything when I was writing this dissertation.

CHAPTER ONE

INTRODUCTION: FROM INORGANIC TO ORGANIC MEMORY

One important part of our life is to remember things because it is directly related to the probability of survival. For example, everybody needs to remember the basic words in his/her language in order to communicate with others. To some degree, a good memory means intelligence. The more you remember, the more powerful you are. Therefore, from the very beginning of human history to now people never stop expanding their brain power using external media to *remember* things. The media varies from stone plate, lamb skin, cloth, and paper to film, tape, disc and finally semiconductor chips. However, only "a device or a component of a device in which information especially for a computer can be inserted and stored and from which it may be extracted when wanted" is defined as "memory", according to the Webster dictionary. Well-known memories in a computer include the CD-ROM, hard disk, floppy disk, and semiconductor-based ROM and RAM. In this dissertation, the topic will be focused on semiconductor memories.

It is the semiconductor memory that made the information age possible. Usually fabricated on a tiny silicon substrate, the semiconductor memory can be found in a lot of modern gadgets today, for example, digital camera, cell phone, MP3 player, key drive,

and, of course, the computer. With the rapid development of technologies, it will not be a surprise that one day we find a memory chip embedded in our clothes or shoes.

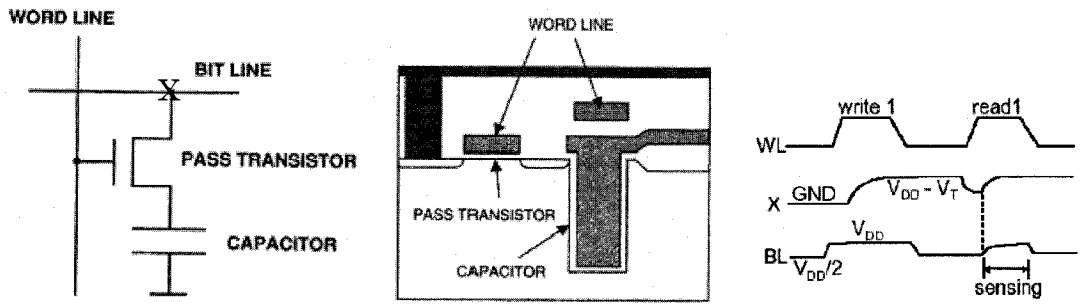
1.1 Traditional Silicon-Based Semiconductor Memory

Silicon-based semiconductor memories fall into two general categories: volatile memory and non-volatile memory.

1.1.1 Volatile Memory: DRAM and SRAM

1.1.1.1 DRAM

DRAM is the abbreviation of Dynamic Random Access Memory. It is the highest density semiconductor integrated circuit (IC) products now and usually used as the indicator of the technology level. With the circuit and cell structure shown in Figure 1.1, a DRAM cell consists of one transistor and one capacitor (1T1C) [1]. Charge is stored in the capacitor. When the capacitor is charged to a "high" voltage, the DRAM cell stores a "1" state; when the capacitor is charged to a "low" voltage, the DRAM cell stores a "0" state.



(a) (b) (c)

Figure 1-1 Circuit (a), structure (b) and write/read operation (c) of a DRAM cell [1].

The write/read operation of DRAM is illustrated in Figure 1-1c. When the wordline (WL) is selected, the data stored on the bitline (BL) will be stored in the capacitor. To read

out the information, BL is pre-charged to $V_{DD}/2$ and WL is selected. As a result, the potential at X will be higher than $V_{DD}/2$ or lower than $V_{DD}/2$ depending on the stored data. A sensing amplifier will detect the potential change.

The electrical charge stored in a DRAM cell gradually discharges, causing the memory cell to lose its information. In order to preserve the information, dynamic memory has to be refreshed periodically by accessing each bit cell at regular intervals. The refresh cycles slow down the operation.

1.1.1.2 SRAM

A SRAM (or static random access memory) cell is a bistable transistor flip-flop, or two inverters connected back to back [1]. The circuit of a full-CMOS 6-transistor SRAM cell is shown in Figure 1-2.

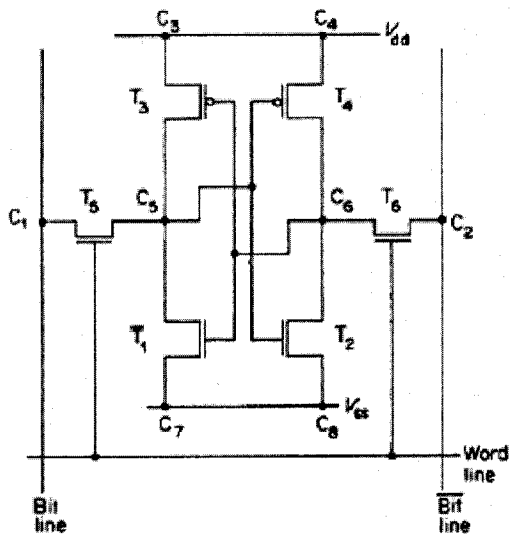


Figure 1-2 Circuit of a CMOS 6-transistor SRAM cell [1].

Write operation (writing "1" as example) is as follows:

- Word line of the cell is selected (raised to V_{DD}, 5V). T_5 and T_6 turn ON.

- Bit-bar line must be forced low. T_1 turns OFF and T_3 turns ON.
- The drain voltage at C_5 rises due to the current flowing through T_5 and T_3.
- When T_2 has been turned ON, the bitline can be returned to its steady level, leaving the cell in the state of storing.

Read operation (reading "1" as example):

- The word line of the cell is selected (raised to V_{DD}). T_5 and T_6 turn ON.
- Both the Bit line and Bit-bar line must be biased at some voltage (e.g., 3 V).
- When the cell is selected, currents flow through T_6 and T_2 to Vss and through T_3 and T_5 to the bitline.
- Since T_2 remaining ON, the voltage of bit-bar line is reduced to < 3 V. While the voltage of bit line is pulled up >3 V since T_1 is OFF but T_3 is ON.
- The differential output signal between the bit and bit-bar lines is fed into the sense amplifier, differential amplifier capable of providing rapid sensing.

SRAM is approximately four or five times faster than DRAM. Since every bit cell requires six or more transistors to function under SRAM, compared to one transistor per bit for DRAM, SRAM modules are relatively larger and more expensive than DRAM.

1.1.2 Non-Volatile Memory

1.1.2.1 ROM

Read-only memory (ROM) is used as a storage medium in computers. Since it cannot, at least not easily, be written to, its main uses lie in the distribution of firmware (software that is very closely related to hardware and does not need frequent upgrading).

Classic mask-programmed ROM chips are written to during production and cannot change content afterwards. It is the most durable form of memory storage. A drawback of

using a mask ROM is the significant cost penalty that must be incurred if an error in the code/data being stored forces a mask set change.

1.1.2.2 EPROM

The first EPROM (Electrically Programmable Read Only Memory), known as the floating gate avalanche-injection metal-oxide-semiconductor memory (FAMOS) [2], was developed using a heavily doped polysilicon (poly-Si) as the floating gate material. The gate oxide thickness was on the order of 100 nm to prevent weak spot or shorting path between the floating gate and the substrate. EPROM was charged by biasing the drain (12.5 V or larger) to avalanche breakdown where the electrons in the avalanche plasma were injected from the drain into the floating gate. The FAMOS could only be erased by ultraviolet (UV) or x-ray. The EPROM was perceived as a tool for system prototyping before a design was committed to Read Only Memory (ROM). Today, one can obtain EPROMs in either a ceramic package with a quartz window that allows for UV exposure or a plastic package without a quartz window. The latter is known as one-time-programmable (OTP) EPROM. The OTP-EPROMs are inexpensive; however, additional testing after assembly is not possible. EPROMs in ceramic packages with a quartz window are expensive but do allow additional testing since the memory can be erased using UV light.

1.1.2.3 EEPROM

In an EEPROM (Electrically Erasable Programmable Read Only Memory), the electrical means is used to restore the charged floating gate to its original uncharged status instead of UV emission approach [3]. Cheaper packaging and a greater ease of use were the first advantages of EEPROMs over their UV-erasable counterparts. The disadvantage of EEPROMs was the cell size that was two to three times the size of an EPROM cell that

resulted in a larger die size. EEPROM cells consist of two transistors, one, a floating gate transistor and the other, a select gate transistor, as shown in Figure 1-3. The select gate transistor is used to select or deselect floating gate transistors for programming or erasing. Die size was further increased to incorporate error correction circuitry or redundancy circuits.

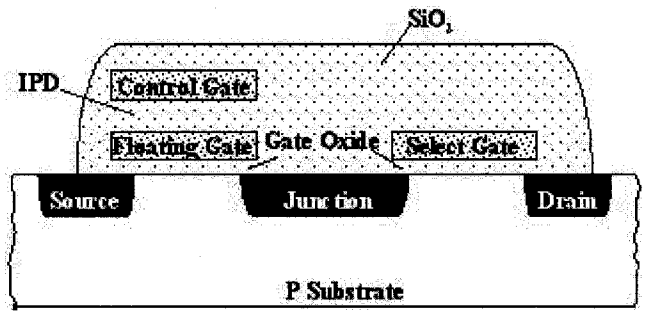


Figure 1-3 An EEPROM cell with select gate transistor.

1.1.2.4 Flash Memory

Flash memory is a form of EEPROM that allows multiple memory locations to be erased or written in one programming operation [4]. It offers fast read access times and solid-state shock resistance.

Figure 1-4a presents a flash memory cell, which looks similar to a standard metal-oxide-semiconductor (MOS) field effect transistor, except that it has two gates instead of just one. One gate is the control gate (CG) like in other MOS transistors, but the second is a floating gate (FG) that is insulated all around by an oxide layer. The FG is between the CG and the substrate. Because the FG is isolated by the insulating oxide layer, any electrons placed on it get trapped there, and thus store the information. When electrons are on the FG, they modify (partially cancel out) the electric field coming from the CG, which modifies the threshold voltage (V_T) of the cell. Thus, when the cell is "read" by placing a

specific voltage on the CG, electrical current will either flow or not flow, depending on the V_T of the cell, which is controlled by the number of electrons on the FG. The presence or absence of current is sensed and translated into 1's and 0's, reproducing the stored data.

A flash memory cell is programmed by starting up electrons flowing from the source to the drain, then a large voltage placed on the CG provides a strong enough electric field to suck them up onto the FG, a process called hot-electron injection (Figure 1-4). To erase, a high electric field (8-10 MV/cm) is present between FG and the channel [5], which drives the electrons out through Fowler-Nordheim tunneling (Figure 1-5).

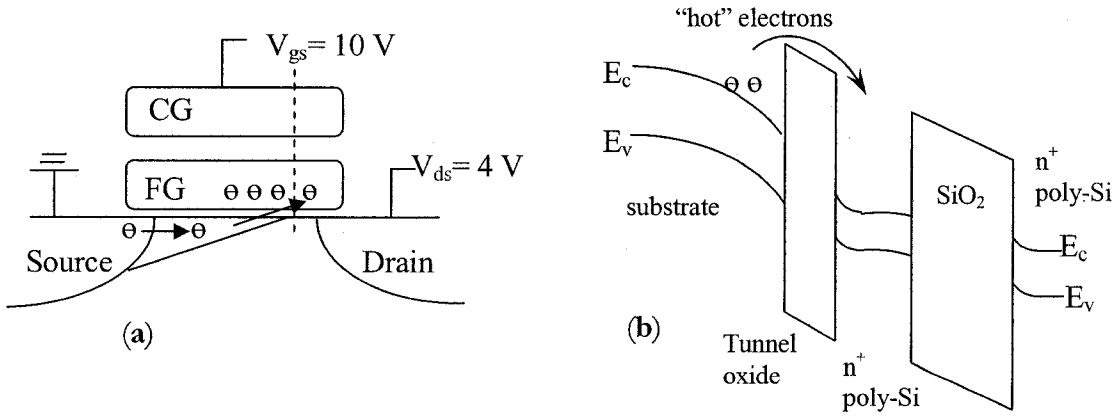


Figure 1-4 (a) Flash memory cell structure with typical biases required for writing into the cell [5]. (b) Energy band diagram along the dashed vertical line in (a) showing channel hot-electron injection.

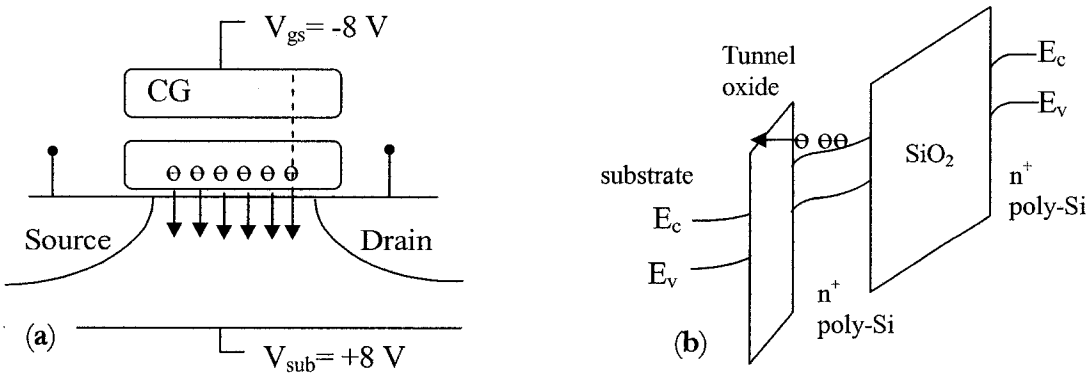


Figure 1-5 Uniform Fowler-Nordheim tunneling to erase flash EEPROM. (a) Cell structure with typical erase bias [5]; (b) Band diagram showing tunneling of carriers from the FG into the oxide.

Most modern flash memory components are divided into erase segments, usually called either blocks or sectors. All of the memory cells in a block must be erased at the same time. Starting with a freshly erased block, any byte within that block can be programmed. However, once a byte has been programmed, it cannot be changed again until the entire block is erased. In other words, flash memory (specifically NOR flash) offers random-access read and programming operations, but cannot offer random-access rewrite or erase operations. When compared to a hard disk drive, a further limitation is the fact that flash memory has a finite number of erase/write cycles, so that care has to be taken when moving hard-drive based applications, such as operating systems, to flash-memory based devices.

1.2 Emerging Inorganic Memory Technologies

The world's appetite for integrated circuit (IC) memory seems to never stop increasing. The consumer's need moved from simple mathematical calculations and word processing that required only kilobits of memory to audio and movie downloads needing gigabytes of memory. Therefore, the semiconductor memory industry has been increasing the memory density for almost three decades, just as predicted by the famous Moore's law, which states that the number of transistors per integrated circuit would double every 18 months. But Moore's law is coming to its end since the IC manufacturing processes (lithography, etching, deposition, etc) are being carried out near their resolution limits. All traditional memories have the scaling limitation and other serious performance limitations mentioned above.

1.2.1 Magnetoresistive RAM

Magnetoresitive random-access memory (MRAM) is a high-speed, nonvolatile memory with unlimited read and write endurance. It combines a magnetic tunnel junction (MTJ) device with standard silicon-based microelectronics. A MTJ is usually constructed using an ultra-thin dielectric layer sandwiched between two ferromagnetic layers. The resistance across the junction is high or low when the magnetic moments of the two ferromagnetic layers are antiparallel or parallel [6].

Figure 1-6 shows the circuit and the cell structure of MRAM. A MRAM cell is composed of one transistor and one MTJ. To write the bit, a current is applied to each write line so that a magnetic field is generated at the bit from both lines simultaneously. To read the data, the isolation transistor is turned on and a current is passed through the MTJ.

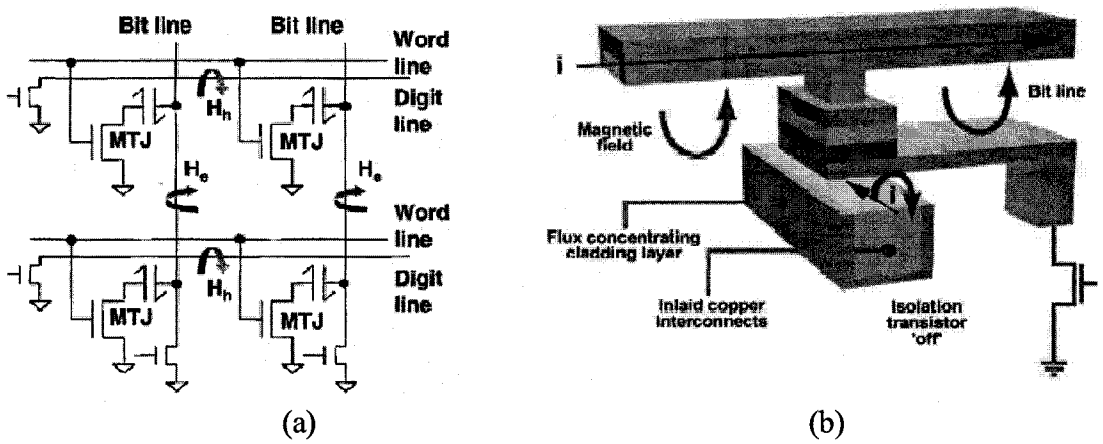


Figure 1-6 Circuit (a) and cell structure (b) of MRAM (courtesy of Motorola).

The key attributes of MRAM are listed as follows:

- High write/read speed competitive with SRAM
- Small size competitive with DRAM
- Nonvolatile with unlimited read-write endurance

- Low leakage and low voltage
- Immunity to soft error and cosmic rays

The MRAM offers multiple memory capabilities that are currently realized only by separate memories. Therefore, it is of potential to replace all the semiconductor memories and become so-called *universal* memory. However, its manufacturing complexity and high cost are still bottle-necks for high-volume production and application.

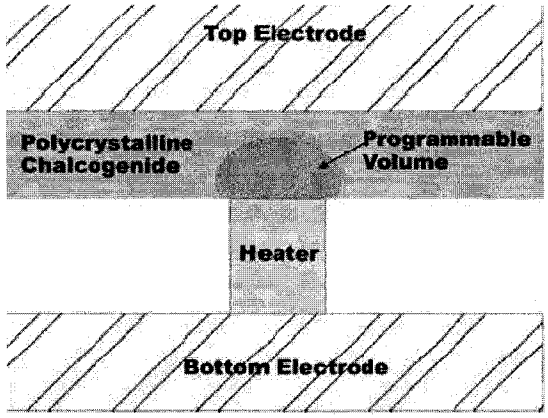
1.2.2 Phase-Change Chalcogenide RAM

Phase-change chalcogenide RAM is based on an electrically initiated, reversible rapid amorphous-to-crystalline phase-change process in multicomponent chalcogenide alloy materials similar to those used in rewritable optical disks [7]. It was first reported by Ovshinsky [8] in 1968. The typical alloy systems include GeSbTe and AgInSbTe. A company named Ovonyx Inc. is now commercializing its phase-change memory technology, called Ovonic Unified Memory (OUM).

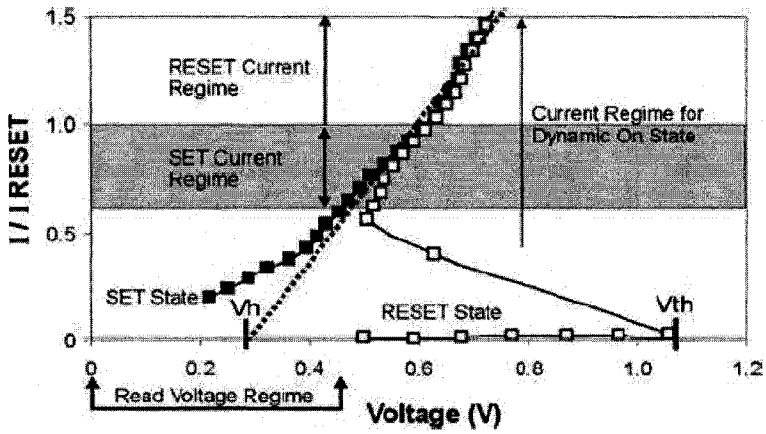
A simplified cell structure of OUM is shown in Figure 1-7a. For a cell in the high-resistance state (RESET), programming to a low-resistance state (SET), as shown in Figure 1-7b, requires a voltage pulse exceeding V_{th}, supplying sufficient dynamic ON-state current to achieve the temperature necessary for crystallization. To switch back, a shorter but higher current pulse is applied to melt the programmed volume of chalcogenide alloy and quench to the amorphous high-resistance state (RESET). In a memory array, MOS transistors or diodes should be used in conjunction with OUM cells to achieve random access.

OUM has some attractive characteristics such as long cycle life, low programming energy and small cell size (less than MRAM cell). These advantages make OUM a

promising candidate to replace flash memory in future applications. The challenge is to demonstrate high volume manufacturability as well as reliability.



(a)



(b)

Figure 1-7 (a) Cross-sectional view and (b) current-voltage (I-V) characteristics of a basic phase-change memory cell [7].

1.2.3 Resistive RAM (RRAM)

The concept of resistive memory is not new. It can be traced back to 1967, when Simmons and Verderber [9] reported resistive memory effects in their Au/SiO/Al devices. The switching of the device involves neither magnetic moment change as in MRAM nor phase change as in OUM.

It is postulated that the injected Au ions introduce a broad band of localized impurity levels within the normally forbidden band of the SiO insulator. The electrons are assumed to move through the insulator by tunneling between adjacent sites within the impurity band. Under certain conditions, e.g., a high voltage pulse, the electrons could be trapped within the impurity band, distort the band structure of the insulator, and thus increase the resistance of the device. The memory state could be read out at a small voltage. Applying a voltage slightly larger than a threshold V_T could drive the trapped electrons out and switch the device back to its low-impedance state [9].

The behavior of the above-mentioned device is called electric bistability, i.e., a phenomenon in which a device exhibits two states of different conductivities at the same applied voltage. This behavior is ideal for memory applications since the memory cell could be constructed using cross-point architecture (Figure 1-8), of which the cell size could be very small, say $4F^2$, as compared to the $6F^2$ of flash memory. Here F refers to feature size.

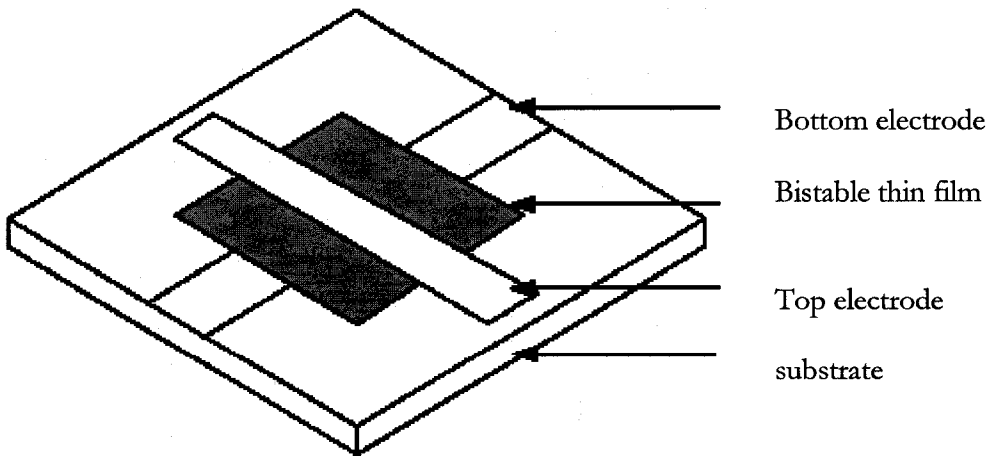


Figure 1-8 The schematic structure of a typical bistable memory cell [10].

Recently, several resistive memory devices have been reported. The active materials include NiO [11-13], TiO_2 [14], $PbTiO_3$ [15], $Pb(Zr_{0.52}Ti_{0.48})O_3$ [16], Cr-doped $SrZrO_3$ [17], $Pr_{0.7}Ca_{0.3}MnO_3$ [18], and $SrTi_{0.99}Nb_{0.01}O_3$ [19, 20]. Samsung Corporation is developing the next-generation nonvolatile memory based on NiO thin films [12, 13], which has shown promising memory properties.

The physical mechanisms of RRAM are still not very clear, although the common driving force—external electric field—is well-known. A few physical models were proposed for the corresponding type of resistive memory elements [21, 22].

1.2.4 Ferroelectric RAM

Ferroelectric random-access memory (FeRAM) uses a ferroelectric thin film as a capacitor for storing data. Currently, PZT [$Pb(Zr_{0.3}Ti_{0.7})O_3$] or SBT ($SrBi_2Ta_2O_9$) is used for commercially available FeRAM. New ferroelectric materials, such as BLT [$(Bi, La)_4Ti_3O_{12}$], have also been developed.

The charge storage of a ferroelectric capacitor is based on the switching of the so-called spontaneous polarization, as shown in Figure 1-9 a. When a sufficiently high electric field is applied between the plates of the capacitor, the ferroelectric film is polarized in one of the two possible net spontaneous polarization states. After the electric field is removed, this electrically written polarization state remains and defines a memory state. Application of an electric field with the same magnitude, but in the opposite direction, causes the capacitor to switch into a *second* stable memory state (Figure 1-9).

The process of electrically defining the orientation of net spontaneous polarization states is the basic physical mechanism used to write and store data in a FeRAM memory.

During the process of switching between the two stable polarization states, an excess charge pulse is drawn from the driving circuit and stored in the capacitor. A FeRAM memory state can be read by detecting the presence or absence of this switching charge pulse when a switching electric field is applied to the ferroelectric capacitor. This read operation is destructive. As a result, refreshing is necessary after each read-out.

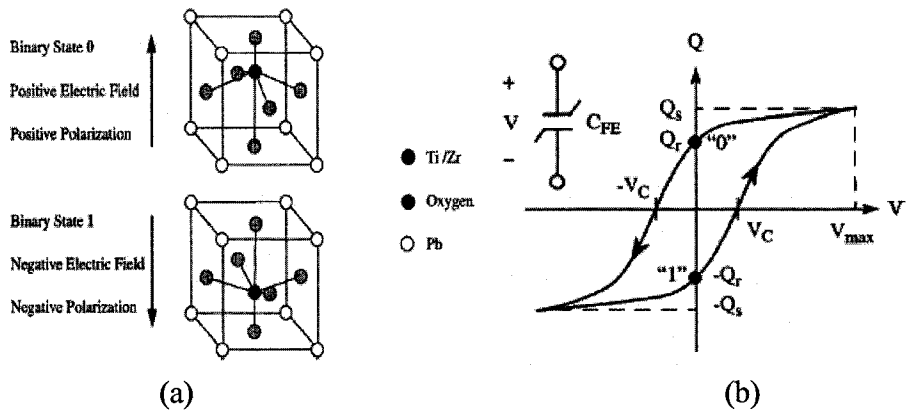
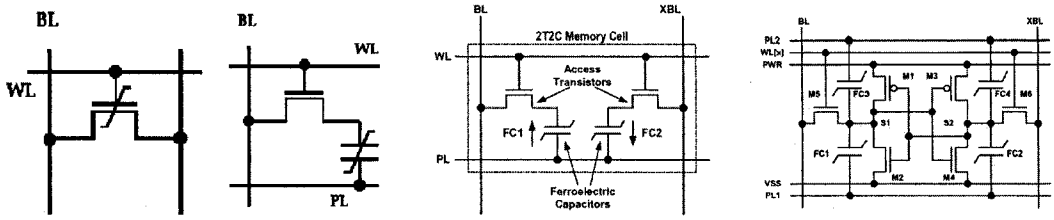


Figure 1-9 (a) Two stable states in a ferroelectric material known as PZT: the orientation of the spontaneous polarization is reversed by applying a proper electric field. (b) Hysteresis loop characteristic of a ferroelectric capacitor. Remanent charge (Q_r), saturation charge (Q_s), and coercive voltage (V_c) are the three important parameters that characterize the loop. The + and - signs beside the capacitor symbol represent the applied voltage polarity [23].

The FeRAM cell architecture inherits from the DRAM, SRAM and flash memories, varying from 1T, 1T1C, 2T2C to 6T4C [24]. The 1T structure has the smallest cell size but shortest data retention time in spite of its non-destructive read operation. The 1T1C and 2T2C cells have acceptable data retention (>10 years), but suffer from the limited read/write endurance due to the destructive read operation. The 6T4C cell exhibits the best performance: access time <10 ns, data retention >10 years, and unlimited endurance to read/write cycling owing to its non-destructive readout [25]. Figure 1-10 illustrates the schematic circuits of above FeRAM cells.



(a) 1T (b) 1T1C (c) 2T2C (d) 6T4C

Figure 1-10 Various types of ferroelectric random-access memory.

FeRAM can achieve high-speed read/write operations comparable to that of DRAM, without losing data when the power is turned off. FeRAM cells offer the advantages of easy embedding into large-scale integration logic circuits and low power consumption (lower than MRAM and OUM).

1.2.5 Nano-Crystal Memory

Nano-crystal memory is a descendent of flash memory. Its write/read/erase operations are very similar to that of flash memory. But the charge is stored in discrete nanoscale particles instead of a whole piece of polysilicon (or nitride) floating gate. Figure 1-11 shows the schematic cross-section of a nano-crystal memory cell.

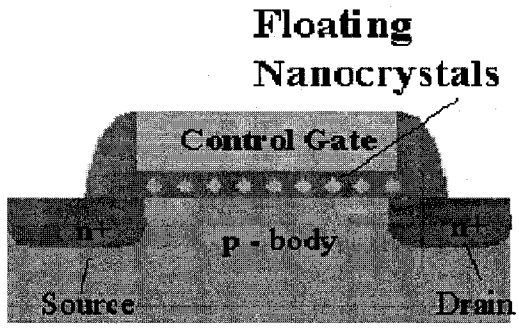


Figure 1-11 A schematic cross-section of the nano-crystal memory cell.

In a nano-crystal memory, the charge loss through lateral paths to the contacting regions is suppressed by use of larger inter-nanocrystal spacing. Thus, smaller oxide

thicknesses (< 5 nm) together with smaller operating voltage become possible [26, 27]. Charge storage in a distributed floating gate of nano-crystals also offers other possible benefits such as small cell size, fast writing, small degradation, and long retention time [27].

Since its debut in 1995 [28], nano-crystal memory has attracted tremendous research efforts. The nano-crystals are usually fabricated by self-assembly methods, of which different approaches were reported [26, 28, 29]. Metal nanocrystals [30-33] and high-κ gate dielectrics [32] were used to improve the device performance.

The ultimate scalability of nano-crystal memory is still limited to many tens of nanometers due to the electrostatic consequences of gate stack thickness, the reduced statistics which directly affect reproducibility, and the constraints of voltages [34]. To keep the scalability going, some new device structures were put forward. Examples include front-defect memories, back-gate memories, and back-trapping memory [34].

1.3 Novel Organic Memory Devices

The last two decades have brought discoveries that small molecules and polymers can be manipulated so that they may be fashioned into transistors, conductors, and other electrical components. A wide variety of potential applications including transistors [35, 36], electronic circuits [37], light emitting diodes [38, 39], and advanced photovoltaic devices [40], have been reported. The benefits of polymers and small molecules are substantial. In many cases, researchers are finding that they offer a safer, cheaper and lighter alternative to silicon. They are cheaper because of the low-cost substrate and large-area capability, lighter due to the plastic substrate instead of silicon, and safer

owing to much less hazardous materials used. Another interesting advantage of organic electronics is the flexibility. For instance, you may roll up a big plastic display and carry it with you.

Figure 1-12 shows the potential market value of organic electronics in 2009. It is not surprising that organic memory accounts for a big part. Everything can become organic. Why not memory? Even so, the organic memory market is only a small section of the whole market of solid state memory, which is predicted to be 153.6 billion dollars in 2010. But the organic part is expanding with the booming of organic electronics.

Currently the organic memories are still in its infant stage. No commercial products have been sold in the market. Nevertheless, the research and development efforts are huge. A lot of papers and patents have been published. According to the device type of memory cell, we can roughly divide the reported organic memories into two categories: the two-terminal resistive memory and the three-terminal transistor memory.

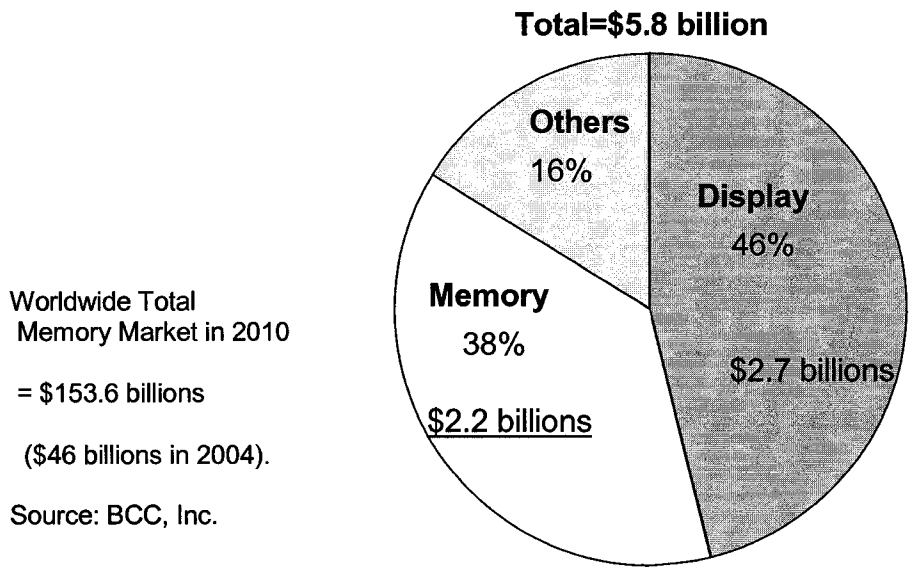


Figure 1-12 Predicted market of organic electronics in 2009. Source: Nano Markets (Feb. 2005). The worldwide memory market data are also presented for comparison.

1.3.1 Organic Resistive Memory

Just like its inorganic counterpart, organic resistive memory is also based on the electrical bistability. However, it is the molecules or polymers that are used as the active materials. The typical organic active materials include charge-transfer complexes, pure small molecules, and polymer/molecule-based composites.

1.3.1.1 Molecular memory

TCNQ (7,7,8,8-tetracyanoquinodimethane) is an organonitrile. Various metals (M) as electron-rich donors can react with TCNQ to form charge-transfer complex M(TCNQ). The metals can be Li, Na, K, Ag, Cu or Fe. Both CuTCNQ and AgTCNQ are frequently investigated [10, 41-43], since they are readily available.

Some organic materials can also form charge-transfer complex with TCNQ. Xu et al. [44] discovered two all-organic complexes, MC+TCNQ and BBDN+TCNQ, with bistable switching effect. (MC is the abbreviation of Melamine Cyanurate, while BBDN is the abbreviation of bis[2-butene-2,3-dithiolato(2-)-*s,s*]-nickel.)

Ma et al. [45, 46] embedded a thin layer of Al nanoclusters in 2-amino-4,5-imidazoledicarbonitrile (AIDCN) thin film and observed encouraging bistability. The structure of an electrical bistable device and the chemical structure of the AIDCN are shown in Figure 1-13. Figure 1-14 shows the typical I-V curves for an AIDCN-based device. Some results are also listed in Table 1-1. One of the most important features is that the initial high impedance state can be recovered by simple application of a reverse voltage pulse. In addition, it was found that the devices remained in the ON-state for several days to weeks.

Al/pentacene/Al also has memory effects [47] with on/off ratio up to 10^9. And the memory effect is dependent on the film thickness. No switching is observed when the film thickness is below 150 nm or above 600 nm. Collier et al. [48] have reported a memory cell using rotaxane, in which the memory effect is caused by the rapid reversible conductance switching of molecules.

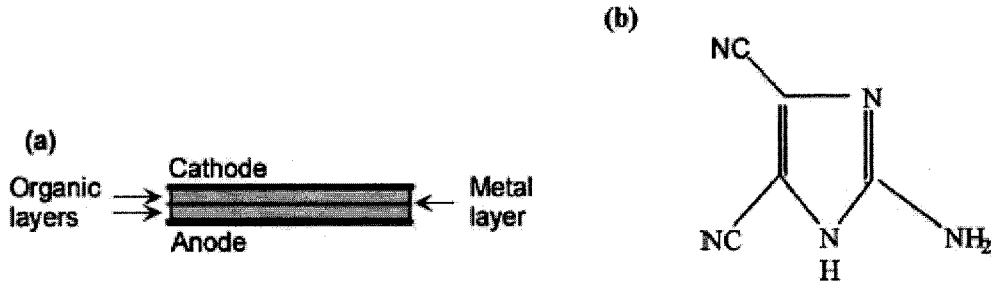


Figure 1-13 (a) The structure of an electrical bistable device and (b) the chemical structure of the organic material [45].

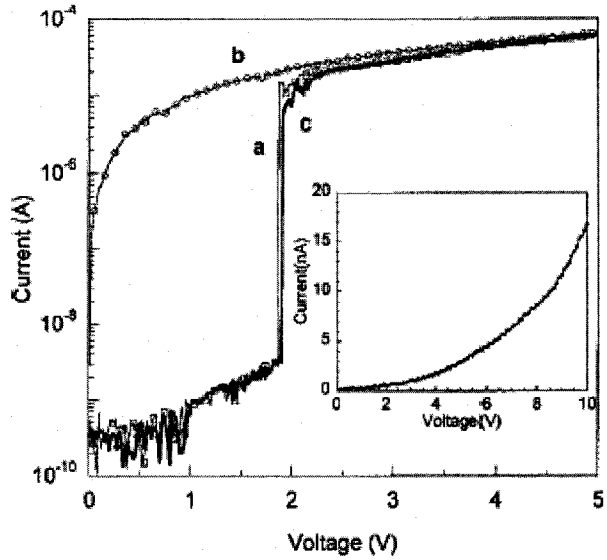


Figure 1-14 I–V characteristics of an organic memory cell with the structure Al/AIDCN(50nm)/Al (20 nm)/AIDCN(50 nm)/Al. Curves (a) and (b) represent the *I–V* characteristics of the first and second bias scan, respectively. Curve (c) is the *I–V* curve of the third bias scan after the application of a reverse voltage pulse (-3 V). The inset shows the *I–V* curves of a device with a 50-nm-thick AIDCN layer as the active medium, where these phenomena can no longer be observed [45].

1.3.1.2 Polymeric memory

Forrest and his co-workers invented a write-once-read-many-times memory using a commercially available polymer PEDOT:PSS (Baytron P) [49]. Sandwiched between ITO and gold electrodes, the thin polymer film can be permanently switched off. Later on, they also reported polymer/silicon hybrid memory cells with lower switch-off voltages [50].

In the last few years, several organic resistive memory devices were reported. It is not necessary to review all of them one by one. Some major progresses made by both the academia and the industry are listed in Table 1-1.

Table 1-1 Summary of organic resistive memories

Typical device	Who/when	mechansim	Advantages	Problems
Cu/CuTCNQ/Al [41]	John Hopkins (1979)	Charge transfer	Easy fabrication	Thermal stability; Not spin-coatable
Al/rotaxane/TiAl [48]	HP (2000)	E-field assisted structure change	Nanometer Scale	Slow L-B deposition Not spin-coatable
Au/PEDOT:PSS/ITO [49]	Princeton (2003)	Carrier injection induced redox	Spin-coating process	Not rewritable, Hard to shrink
Al/NanoAu-PS/Al [51]	UCLA (2004)	Charge-transfer	Spin-coating process	
Al-AIDCN/Al/AIDCN-Al [45]	UCLA (2002)	Charge storage	Fast	Vacuum deposit Not spin-coatable
Al-AIDCN/Cr/AIDCN-Al [52]	IBM (2004)	Charge storage	Fast	Similar as above
Al-C/polyester-Ag	MIT (2000)	Not disclosed	Cheap, printable	30min retention Hard to shrink
Ti/Ag2S/polydiphenyl-acetylene/a-C	Coatue Co. (2002)	E-field assisted doping	Cheap, printable	Cycle life Hard to shrink

1.3.2 Organic Transistor Memory

For the sake of simplicity, the recent development of organic field effect transistor (OFET) memory is summarized in Table 1-2. It seems that all the OFET memory reported so far are based on the ferroelectric (or ferroelectric-like) behavior of the gate dielectric. It

should be noted that the claimed all-organic is not really 'ALL' organic in nature since the electrode materials are still metals.

Table 1-2 The OFET memory devices reported in literature

Typical device	Who/when	Mechanism	Advantages	disadvantages
OFET with MXD6 as gate dielectric [53]	U. Sheffield (2005)	Polarization of ferroelectric polymer	Cheap; Solution-processable	High switch voltage
OFET with PVDF/TrFE as gate dielectric [54]	Xerox Co. (2002)	Polarization of ferroelectric polymer	Cheap; Solution-processable	High switch voltage
OFET with PVA as gate dielectric [55]	Johannes Kepler U. (2004)	charge storage in electret polymer	Cheap; Solution-processable	High switch voltage

1.3.3 Other Organic Memories

Hybrid CMOS/molecular memory devices [56, 57] have been demonstrated by a group from the University of California at Riverside and North Carolina State University. Based on DRAM architecture, the devices have high density, and exhibit low power consumption. Each memory cell contains a monolayer of molecules such as porphyrin or ferrocene to store charge. The oxidation state of porphyrin molecules produces charge states analogous to a DRAM capacitor. Their main advantages over traditional DRAM are:

(1) High charge density (10 times larger);

(2) Longer charge retention (10000 times longer);

(3) Multiple bits per cell;

(4) Scalable to near-molecular dimensions.

Unfortunately, the operation is rather slow (a few milliseconds), due to the presence of a large liquid solution resistance component.

Carbon nanotubes were used to construct cross-point memory cells based on the their electromechanical deformation [58]. A MEMS based memory was also reported [59] and is being commercialized. An array of AFM cantilever beams are used to make marks (with the AFM tips) on the substrate (usually plastic) for information storage.

1.4 Dissertation Objective

From the above review, we can see problems associated with the reported organic memories. For the organic resistive memory, the issues lie in the scalability, the reliability and the cost. For example, Ma's molecular memory [45] is fabricated under vacuum environment, which will raise the cost. Möller's polymer memory [49] is hard to scale down. In the case of the transistor memory, the major problem is the high operational voltage.

The ideal memory subsystem optimizes density, preserves critical information in a nonvolatile condition, is easy to program and reprogram, can be read fast, and is cost-effective for the application. Can we make an organic memory meeting all the requirements above? For the time being we cannot answer "absolutely". But a least we can say "possibly". The purpose of this work is to explore the possibility of such kind of organic memories, while focusing on the low-cost aspects. As a colleague once explained, there are three factors that drive memory: cost, cost, and cost. The detailed objectives of this dissertation are:

(1) to design, fabricate, and characterize organic resistor and diode memory devices which is both solution-processable and shrinkable;

(2) to design, fabricate, and characterize an OFET memory which can be, at least potentially, operated at low voltages;

(3) to develop physical models for the above memories;

(4) to simulate and optimize the memory devices using TCAD tools.

1.5 Dissertation Outline

This dissertation is focused on the design, modeling and simulation, fabrication, and characterization of organic non-volatile memory devices. Three types of memory devices, resistor type, diode type and transistor type, are investigated.

Chapter Two describes the physics of organic memory devices. First, the mechanisms of charge transport in organic semiconductors and dielectrics are described. Then, the memory effect based on charge storage model is theoretically discussed for both diode memory and transistor memory.

Chapter Three presents the experimental methods used to fabricate and characterize the memory devices. The fabrication involves deposition of organic thin films using spin-coating and inkjet printing, deposition of metal nanoparticle film using Layer-by-Layer self-assembly, modification of film surface using self-assembled monolayer. Electrical characterization of the final devices will be discussed.

Chapter Four demonstrates an organic resistive memory devices based on a spin-coated organic molecular complex film PCBM/TCNQ. When the complex film containing molecular nanodots is sandwiched between two metal electrodes, it exhibits memory effects. The fabrication processes, characterization results, and explanations are given in this chapter.

Chapter Five illustrates an improved version of the memory devices mentioned in Chapter Four. A p-type semiconductor polymer PEDOT:PSS is used to form p^+-N heterojunction with PCBM/TCNQ. The heterojunction diode exhibits rewritable memory

effects. A charge storage model is proposed to explain the current-voltage characteristics and the memory behavior. The model is qualitatively verified with 2D simulation using TCAD tool Taurus–Medici.

Chapter Six presents a nanodot transistor-type memory device based on an organic thin film transistor. Gold nanoparticles are integrated in the gate dielectric for charge storage. The memory effect of the charge storage is verified with 3D device simulation using Taurus-Tsuprem4 and Taurus-Medici. Device fabrication procedure, measurement results and relevant trapping effects are described and discussed.

Chapter Seven summarizes the dissertation and presents suggestions for the future work.

CHAPTER TWO

THEORETICAL BACKGROUND OF ORGANIC MEMORY

2.1 Organic Semiconductors

2.1.1 Basic Concept—Conjugation

Semiconductors based on organic molecular components have been the focus of intense investigation for the past half century. During most of that time, these materials, primarily consisting of C, H, and O were considered to be merely a scientific curiosity. The solid state structure of these materials is based on individual molecular components bound together by weak interactions, principally van der Waals and dipole-dipole forces, imparting within them the properties of both semiconductors and insulators [60].

Up to now, a number of classes of organic semiconductors have been discovered, ranging from small molecules based on (hetero) aromatic rings, conjugated polymers, and hybrid organic-inorganic structures, to truly molecular semiconductors such as buckyballs and nanotubes. The chemical structure and electrical properties of some common organic semiconductors can be found in Appendix I. All these structures exhibit the common feature of having *conjugated bonds*, in which the presence of mobile (highly polarizable) π-electrons has a dramatic impact on the potential electrical performance. This situation is reversed compared to non-conjugated or all-σ compounds, such as polyethylene and

Teflon, which are excellent insulators [61]. Figure 2-1 shows some examples of these systems.

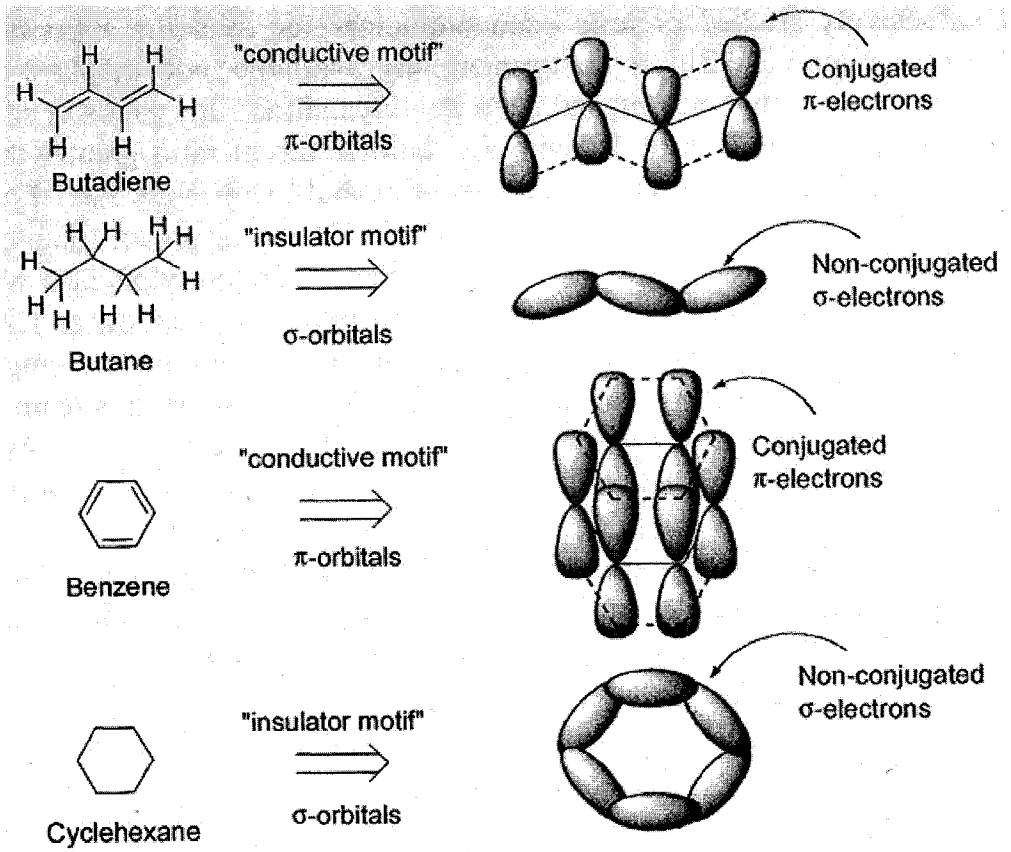


Figure 2-1 π-conjugated and non-conjugated molecules [61].

2.1.2 Charge Carriers in Organic Semiconductors

Organic semiconductors can also be p-type (or n-type) doped by (1) adding external electron acceptor (or donor); (2) incorporating specific (e.g., electron-withdrawing) chemical groups into the molecular structure. The vast majority of the organic semiconductors exhibit p-type conductivity. The number of high efficiency n-type organic semiconductors is extremely limited because these unique materials have a propensity to degrade upon exposure to atmospheric conditions. Typically, n-type organic

semiconductors oxidize when exposed to oxygen and the negative charge carriers within the materials are lost. Incorporation of strong electron-withdrawing chemical groups, for example, –F and –CN, into the molecular structure results in some air-stable n-type organic semiconductors such as $F_{16}CuPc$, F_4TCNQ, and PCBM. This is reminiscent of doping of silicon based semiconductors where silicon is doped with either arsenic or boron. However, while the doping of silicon produces a donor energy level close to the conduction band or an acceptor level close to the valence band, this is not the case with conducting polymers. The evidence for this is that the resulting polymers do not have a high enough concentration of free spins, as determined by electron spin spectroscopy. Initially the free spins concentration increases with concentration of dopant. At larger concentrations, however, the concentration of free spins levels off at a maximum.

To understand this, it is necessary to examine the way in which charge is stored along the polymer chain and its effect. The polymer may store charge in two ways. In an oxidation process it could either lose an electron from one of the bands or it could localize the charge over a small section of the chain. Localizing the charge causes a local distortion due to a change in geometry, which costs the polymer some energy. However, the generation of this local geometry decreases the ionization energy of the polymer chain and increases its electron affinity making it more able to accommodate the newly formed charges. This method increases the energy of the polymer less than it would if the charge was delocalized and, hence, takes place in preference of charge delocalization. This is consistent with an increase in disorder detected after doping by Raman spectroscopy. A similar scenario occurs for a reductive process.

Typical oxidizing dopants include iodine, arsenic pentachloride, and iron (III) chloride. A typical reductive dopant is sodium naphthalide. The main criteria is its ability to oxidize or reduce the polymer without lowering its stability or whether or not they are capable of initiating side reactions that inhibit the polymers ability to conduct electricity. An example of the latter is the doping of a conjugated polymer with bromine. Bromine is a strong oxidant and adds across the double bonds to form sp^3 carbons.

The oxidative doping of polypyrrole proceeds in the following manner. An electron is removed from the π-system of the polymer backbone producing free radical and a spinless positive charge. The radical and cation are coupled to each other via local resonance of the charge and the radical. In this case, a sequence of quinoid-like rings is formed. The distortion produced by this is of higher energy than the remaining portion of the chain. The creation and separation of these defects costs a considerable amount of energy. This limits the number of quinoid-like rings that can link these two bound species together. In the case of polypyrrole, it is believed that the lattice distortion extends over four pyrrole rings. This combination of a charge site and a radical is called a polaron. It could be either a radical cation or radical anion. It creates a new localized electronic state in the gap, with the lower energy states being occupied by a single unpaired electron. The polaron states of polypyrrole are symmetrically located about 0.5 eV from the band edges. Upon further oxidation the free radical of the polaron is removed, creating a new spinless defect called a bipolaron. Formation of a bipolaron is of lower energy than the creation of two distinct polarons. At higher doping levels it becomes possible that two polarons combine to form a bipolaron. Thus at higher doping levels the polarons are replaced with bipolarons. The bipolarons are located symmetrically with a band gap of 0.75 eV for

polypyrrole. This eventually, with continued doping, forms into a continuous bipolaron bands. Their band gap also increases as newly formed bipolarons are made at the expense of the band edges. For a very heavily-doped polymer, it is conceivable that the upper and the lower bipolaron bands will merge with the conduction and the valence bands, respectively, to produce partially filled bands and metallic-like conductivity. This is shown in Figure 2-2.

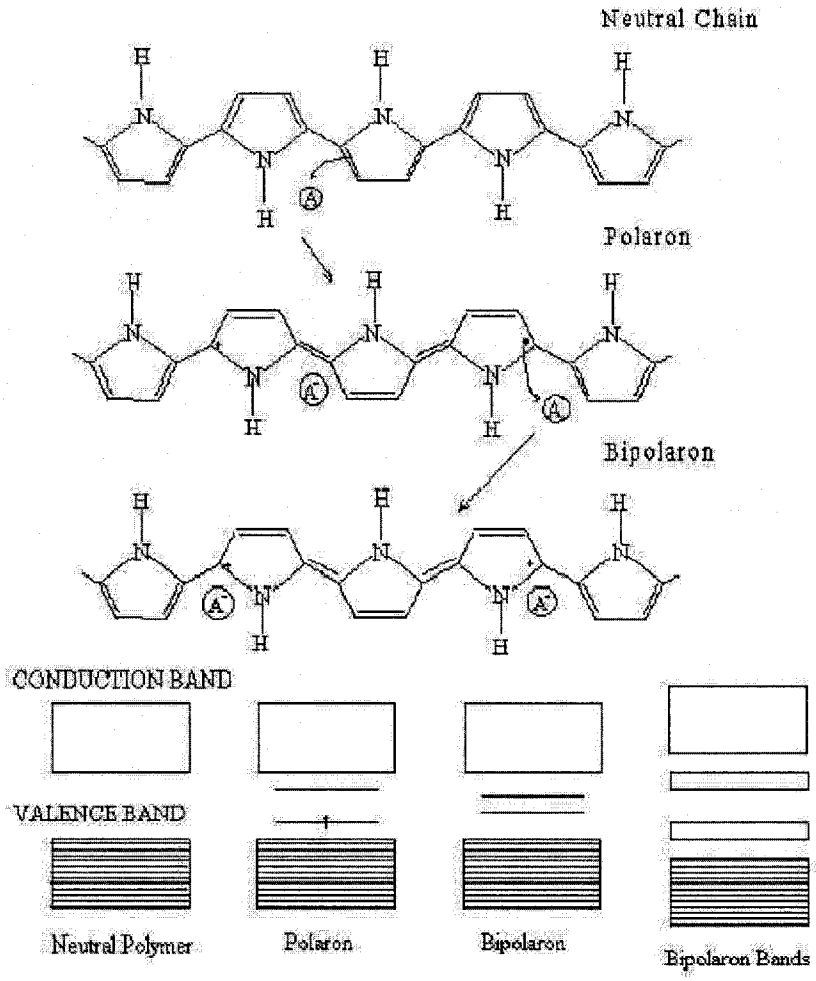


Figure 2-2 Polaron and bipolaron in polypyrrole chain.

Conjugated polymers with a degenerate ground state have a slightly different mechanism. As with polypyrrole, polarons and bipolarons are produced upon oxidation.

However, because the ground state structure of such polymers are twofold degenerate, the charged cations are not bound to each other by a higher energy bonding configuration and can freely separate along the chain. The effect of this is that the charged defects are independent of one another and can form domain walls that separate two phases of opposite orientation and identical energy. These are called solitons and can sometimes be neutral. Solitons produced in polyacetylene are believed to be delocalized over about 12 CH units with the maximum charge density next to the dopant counterion. The bonds closer to the defect show less amount of bond alternation than the bonds away from the defect. Soliton formation results in the creation of new localized electronic states that appear in the middle of the energy gap. At high doping levels, the charged solitons interact with each other to form a soliton band which can eventually merge with the band edges to create true metallic conductivity.

2.2 Charge Transport in Organic Semiconductors

2.2.1 Intramolecular Transport

Theoretically, charge transport through a single molecule or conjugated polymer chain could be ballistic, in that no resistive energy is dissipated on the molecule, as has been described for nanosized silicon transistors, carbon nanotubes, and a wide variety of other inorganic semiconductor devices [62]. Charge would merely have to hop twice, from a contact to a single orbital and then out to another contact again. The realization of such kind of single molecular devices is still elusive [63].

Two major obstacles to observing *single molecule* mobility are the frequently encountered contact resistance at the metal-molecule junction and a defective molecular structure that could include twists and oxidized sites that interrupt the conjugation.

2.2.2 Intermolecular (or Interchain) Transport

Organic solids are specific in several respects. The basic feature distinguishing these solids from their standard inorganic counterparts is the fact that the main building units are organic molecules which, in the condensed matter state, preserve their physical identity well. Atoms in the individual molecules are bound by forces which have mostly a *covalent* character. But the binding forces among the molecules are usually of the *van der Waals* type. Therefore, the molecules keep behaving as though they were in a gas phase even in a perfect molecular crystal. This consequently leads to a marked tendency for *localization* of charge carriers on individual molecules. Although the band-like charge transport was observed in some molecular crystals and even polycrystalline thin films [64], the carriers' motion in most organic semiconductors should be described as "hopping transport", a phonon-assisted tunneling mechanism from site to site. In disordered organic semiconductors, the hopping rate, k_{ET}, can be described with a good approximation as [65]

$$k_{ET} = \frac{4\pi^2}{h}\frac{1}{\sqrt{4\pi k_B T}}t^2 \exp\left(-\frac{\lambda}{4k_B T}\right) \qquad (2\text{-}1)$$

where T is the temperature, λ is the reorganization energy, t is the transfer integral, and h and k_B are the Planck and Boltzmann constants, respectively. The transfer integrals reflect the strength of the interaction between the two molecules; the reorganization energy term describes the strength of the electron-phonon (vibration) interaction and can be reliably estimated as twice the relaxation energy of a polaron localized over a single unit.

Equation (2-1) tells us that the hopping rate is exponentially related to the energy required to vibrate the molecule for transferring a polaron. The less energy is required, the easier the polaron to be transported. It also tells us that the hopping rate first increases

with temperature when the $\exp(-\frac{\lambda}{4k_BT})$ term dominates and then decreases when the $\frac{1}{\sqrt{4\pi k_BT}}$ term dominates because $\exp(-\frac{\lambda}{4k_BT}) \rightarrow 0$ when T$\rightarrow$ infinite.

The carrier transport in polymer semiconductors is similar. The polymer chain can be seen as a sequence of relatively short conjugated segments of varying length. In this "molecular" picture, excitations and/or charge are localized on such segments (called as sites). Because of the variation in conjugation lengths, the energy levels are distributed. Charge transport in such systems, being the result of interchain (intersite) hopping, has been studied in great detail during the last decade. The accepted picture is hopping transport between the elementary sites possessing energetic and positional disorder. The hopping rate can be described using Miller-Abrahams [66, 67] approximation:

$$P_{i\to j} = \exp(\gamma \frac{R_{ij}}{a}) \exp(-\frac{E_j - E_i}{kT}) \exp[\frac{F(x_j - x_i)}{kT}] \qquad (2\text{-}2)$$

where γ is the tunneling rate, R_{ij} distance between sites, a lattice unit size, E_i site energy, k Boltzman's constant, T temperature, F electric field, $(x_i\text{-}x_j)$ displacement along field. This equation indicates that the interchain hopping rate exponentially increases with the electric field. The effect of temperature is similar to that in Equation (2-1), depending on which term is dominant, $\exp(-\frac{E_j - E_i}{kT})$ or $\exp[\frac{F(x_j - x_i)}{kT}]$.

2.2.3 Intergrain Transport

Just like in inorganic semiconductors, grain boundaries are energy barriers limiting the mobility in almost all organic semiconductor films. The mechanism by which charge transport is hindered by grain boundaries can be described by viewing the grain boundary either as a site of repelling potential [68] or as a trap [69, 70] (Figure 2-3).

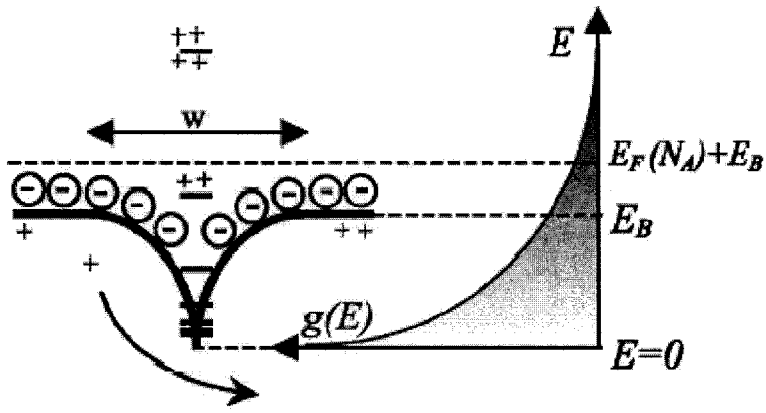


Figure 2-3 Hole transport band of a polycrystalline semiconductor [70].

According to Verlaak et al. [70], the intergrain barrier shown in Figure 2-3 can be expressed as

$$E_B = \frac{q^2\Sigma^2}{8\varepsilon N_a}, \tag{2-3}$$

where Σ is the trapped charges per unit interfacial area, which can be described as

$$\Sigma = \int_0^\infty \frac{g(E)}{1+\exp(\frac{E_B + E_F - E}{kT})} dE. \tag{2-4}$$

Here in Equation (2-4) g(E) is the distribution of localized states, EF is the Fermi energy level determined by the acceptor-like dopant concentration N_a.

The mobility in a polycrystalline organic semiconductor film is controlled by the rate of thermionic carrier jump across the grain boundary as

$$\mu \approx \mu_0 \exp(-\frac{E_B}{kT}) \tag{2-5}$$

with μ_0 linearly increasing with grain size. Equation (2-3) shows that higher dopant concentrations screen the charges at the grain boundary more effectively and the barrier is lower.

2.3 Electric Current through Insulators and Semiconductors

Charge transport through semiconductors and insulators may involve the following mechanisms: ballistic transport, Fowler-Nordheim Tunneling, Poole-Frenkel emission, as well as space charge effects.

2.3.1 Ballistic Transport

Ballistic transport is carrier transport without scattering or any other mechanism, which would cause a loss of energy. Ballistic transport is seen in nanosized silicon field effect transistors [71] and carbon nanotubes [62]. Combining energy conservation, current continuity and Gauss's law one finds the following current-voltage relationship for a metal/semiconductor/metal structure [72]:

$$J = \frac{4\varepsilon}{9}\sqrt{\frac{2q}{m^*}}\frac{V^{3/2}}{d^2} \tag{2-6}$$

where d is the thickness of the material and m^* is the effective mass of the carriers.

2.3.2 Fowler-Nordheim Tunneling

Fowler-Nordheim tunneling has been studied extensively in metal-oxide-semiconductor structures where it has been shown to be the dominant charge transport mechanism, especially for thick oxides. The basic idea is that quantum mechanical tunneling from the adjacent conductor into the insulator limits the current through the structure. Once the carriers have tunneled into the insulator they are free to move within the valence or conduction band of the insulator. The calculation of the current is based on the Wentzel-Kramers-Brillouin (WKB) approximation yielding the following relation [73, 74] between the current density, J_{FN}, and the electric field in the insulator, E:

$$J_{FN} = C_{FN}E^2 \exp\left(-\frac{4}{3}\frac{\sqrt{2m^*}}{q\hbar}\frac{(q\phi_B)^{3/2}}{E}\right) \tag{2-7}$$

where ϕ_B is the barrier height at the metal/insulator interface in Volt. To check for this current mechanism, experimental *I-V* characteristics are typically plotted as $ln(J_{FN}/E_{ox}{}^2)$ versus $1/E_{ox}$, a so-called Fowler-Nordheim plot. Provided the effective mass of electrons in the insulator is known (for SiO_2, $m_{ox}^* = 0.42\ m_0$), one can then fit the experimental data to a straight line yielding a value for the barrier height [72].

It is this type of measurement which has yielded experimental values for the conduction band difference between silicon and silicon-dioxide. The same method could also be used to determine heterojunction energy band off-sets provided Fowler-Nordheim tunneling is indeed the dominant current mechanism. It is important to stress that carriers must tunnel through the insulator (or semiconductor), which requires: $E \cdot d \geq \phi_B$, which is typically the case for thick oxides and high electric fields.

2.3.3 Poole-Frenkel Emission

The expression for Fowler-Nordheim tunneling implies that carriers are free to move through the insulator or semiconductor. Whereas this is indeed the case in thermally-grown silicon-dioxide, it is frequently not so in deposited materials which contain a high density of structural defects. Silicon nitride (Si_3N_4) is an example of such material. The structural defects cause additional energy states close to the band edge called traps. These traps restrict the current flow because of a capture and emission process, thereby becoming the dominant carrier transport mechanism, which is named after its theoretical founders Poole and Frenkel [75]. The current is a simple drift current described by

$$J = qn\mu E \tag{2-8}$$

where μ is the carrier mobility, n is the carrier density depending exponentially on the

depth of the trap ϕ_{PF} which is corrected for the electric field E [76]:

$$n = n_0 \exp[-\frac{q}{kT}(\phi_{PF} - \sqrt{\frac{qE}{\pi\varepsilon}})] \tag{2-9}$$

The total current then equals:

$$J_{PF} = qn_0\mu E \exp[-\frac{q}{kT}(\phi_{PF} - \sqrt{\frac{qE}{\pi\varepsilon}})] \tag{2-10}$$

The existence of a large density of shallow traps in CVD (chemical vapor deposition) silicon nitride makes Poole-Frenkel emission a frequently observed and well-characterized mechanism.

2.3.4 Space Charge Limited Current

Both Fowler-Nordheim tunneling and Poole-Frenkel emission mechanisms yield very low current densities with correspondingly low carrier densities. For structures where carriers can readily enter the insulator and freely flow through the insulator one finds that the resulting current and carrier densities are much higher. The high density of free carriers causes a field gradient, which limits the current density. This situation occurs in lightly doped semiconductors and vacuum tubes. Starting from an expression for the drift current $J = qn\mu E$ and Gauss's law

$$\frac{dE}{dx} = \frac{qn}{\varepsilon} \tag{2-11}$$

We can eliminate the carrier density, n, yielding:

$$\frac{J}{\varepsilon\mu} = E\frac{dE}{dx} \tag{2-12}$$

Integrating this expression from 0 to x, where we assume the electric field to be zero for ideal ohmic contact at $x = 0$, one obtains:

$$\frac{Jx}{\varepsilon\mu} = \frac{E^2}{2} \tag{2-13}$$

or

$$E(x) = \sqrt{\frac{2xJ}{\varepsilon\mu}} \tag{2-14}$$

Integrating once again from $x = 0$ to $x = d$ with $V(0) = V$ and $V(d) = 0$, one finds:

$$V = \int_0^d E dx = \sqrt{\frac{2J}{\varepsilon\mu}} \frac{d^{3/2}}{3/2} \tag{2-15}$$

from which one obtains the expression for the space-charge-limited current:

$$J = \frac{9\varepsilon\mu V^2}{8d^3} \tag{2-16}$$

In equation (2-16), the current density is directly proportional to the mobility and to the square of the applied voltage, and inversely proportional to the cube of the film thickness between two electrodes.

2.4 Charge Storage and Transport in Organic Diodes

2.4.1 Metal-Organic-Metal Diode

The current through a metal-organic-metal (MOM) diode may obey one of the above equations, depending on the properties of the metals and organic materials. In a MOM diode, the energy barrier (metal-organic) and carrier concentration are two key factors that affect the diode current.

If charge traps are intentionally introduced into the diode, they will store charges when the current flows through the diode upon external bias. On one hand, those trapped charges can distort the energy bands of the organic film and influence the energy barrier at

metal-organic interface (Figure 2-4). On the other hand, the electric field induced by trapped charges may also change the hopping rate of carriers in the surrounding regions, according to Equation (2-2). In any case, the conductance of the device may significantly change, producing interesting memory effects.

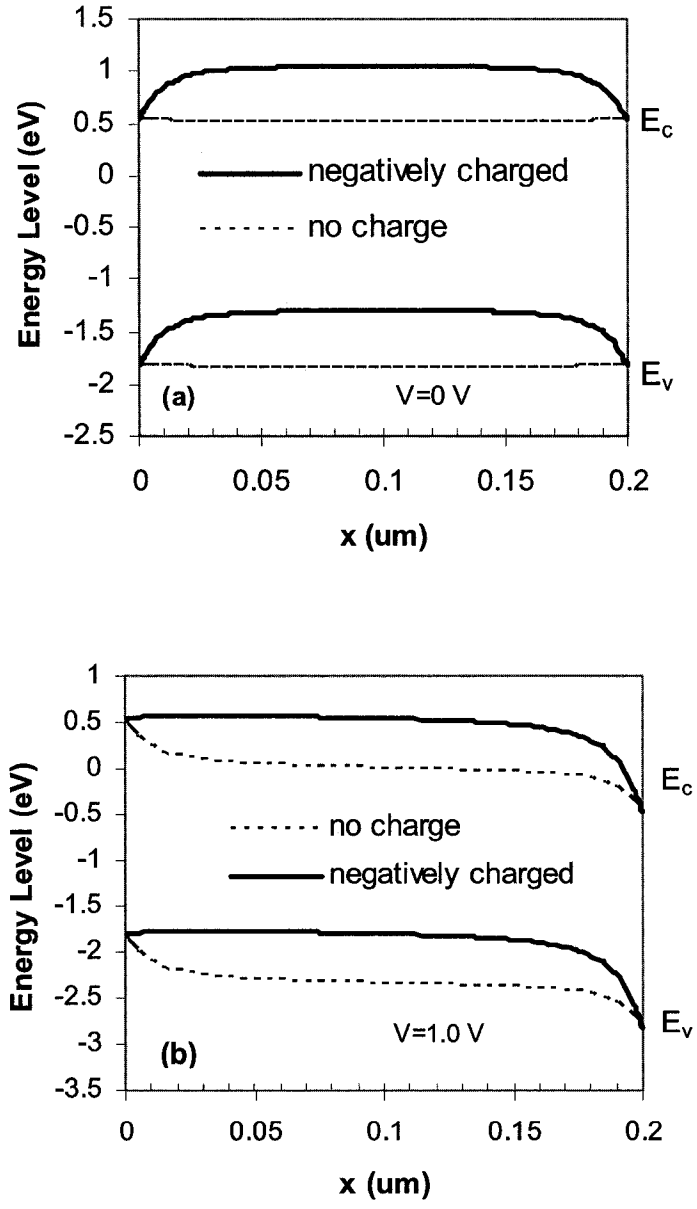


Figure 2-4 Energy band diagrams distorted by trapped negative charges in the organic film under zero bias (a) and 1.0 V bias (b). Zero energy level refers to Fermi level.

2.4.2 Organic Heterojunction Diode

Charge storage in an organic heterojunction can result in similar effects mentioned above. For example, the charge trapped in the N-region of a p^+-N heterojunction could bend up the energy band edges and significantly lower the built-in potential barrier, as shown in Figure 2-5, so as to change the current-voltage characteristics of the diode. In Chapter Five, an organic diode memory device is demonstrated based on this principle.

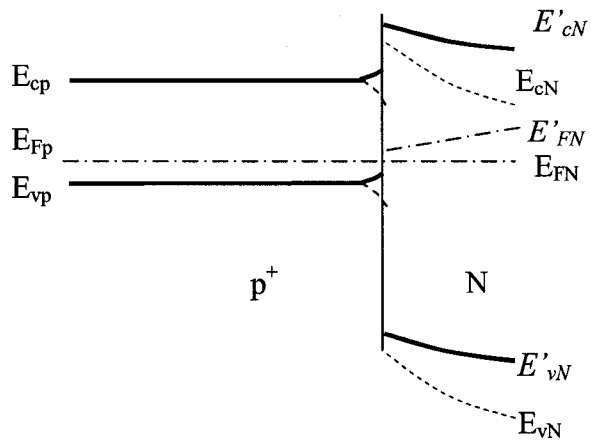


Figure 2-5 Ideal energy-band diagram of p^+-N heterojunction before (dashed line) and after (solid line) negative charge storage at N side.

2.5 Charge Storage in the Floating Gate of an Organic Transistor

2.5.1 Organic Thin Film Transistors with Nanodot Floating Gate

The schematic structure of the transistor memory is shown in Figure 2-6a. The channel material is a conjugated polymer. Regioregular poly(3-hexylthiophene) (rr-P3HT) is used for this work. Metal nanoparticles are integrated into the gate dielectric layer as the floating gate. Although the ultimate goal is to fabricate a low-cost all-organic OTFT memory, a less difficult approach would be a hybrid version with SiO_2 as the control gate dielectric.

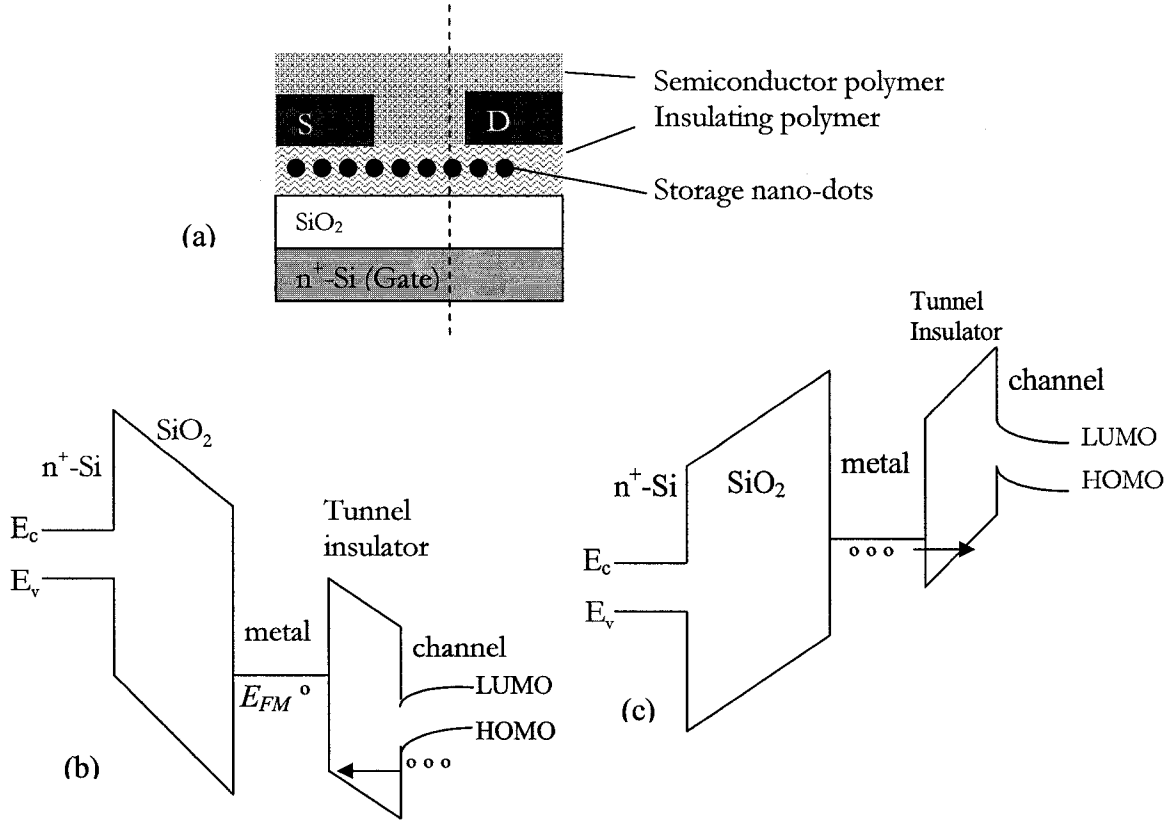


Figure 2-6 Schematic structure (a) and energy band diagrams of write (b) and erase (c) operations of the p-channel organic transistor memory device.

2.5.2 Basic Operation for Charge Storage

The principle of the transistor memory device in this work is very similar to that of the traditional nano-crystal memory. The difference lies in the low mobility of organic semiconductor materials. From $v = \mu E$, the velocity v of carriers in an OTFT should be four orders of magnitude smaller than that in a Si-based transistor, assuming the mobility of organic semiconductor is at the level of 0.01 $cm^2 \cdot V^{-1} \cdot s^{-1}$. As a result, there are few hot electrons or holes in the channel to inject into the floating gate of an OTFT. Hence, the write/erase mechanisms of an OTFT memory should be basically F-N tunneling.

Figure 2-6b and c illustrate the energy band diagrams along the dashed line in Figure 2-6a during the write operation and erase operation, respectively. When the writing operation is carried out, the gate is negatively biased. The holes are accumulated at the interface between the tunnel insulator and the channel. The high electric field results in the F-N tunneling of holes through the tunnel insulator to potential wells—the metal nanodots. To erase the information, the holes stored in the metal nanodots are driven out to the channel by applying a positive gate voltage.

CHAPTER THREE

EXPERIMENTAL METHODS

3.1 Device Fabrication Techniques

3.1.1 Spin-Coating Technique

Spin-coating has been used for several decades for the application of thin films. A typical process involves depositing a small puddle of a fluid solution onto the center of a substrate and then spinning the substrate at high speed (typically around 3000 rpm). Centrifugal acceleration will cause the solution to spread to, and eventually off, the edge of the substrate leaving a thin film on the surface. Final film thickness and other properties depend on the nature of the solution (viscosity, drying rate, solid content, surface tension, etc.) and the parameters chosen for the spin process. Factors such as final rotational speed, acceleration, and fume exhaust contribute to how the properties of coated films are defined.

For most resin materials the final film thickness will be inversely proportional to the spin speed and spin time. Final thickness will also be somewhat proportional to the exhaust volume although uniformity will suffer if the exhaust flow is too high since turbulence will cause non-uniform drying of the film during the spin-coating process.

3.1.1.1 Spin-coating process stages

As shown in Figure 3-1, the spin-coating process can be divided into four stages. The first stage is the deposition of the coating fluid onto the wafer or substrate. The second stage is when the substrate is accelerated up to its final, desired, rotation speed. This stage is usually characterized by aggressive fluid expulsion from the wafer surface by the rotational motion.

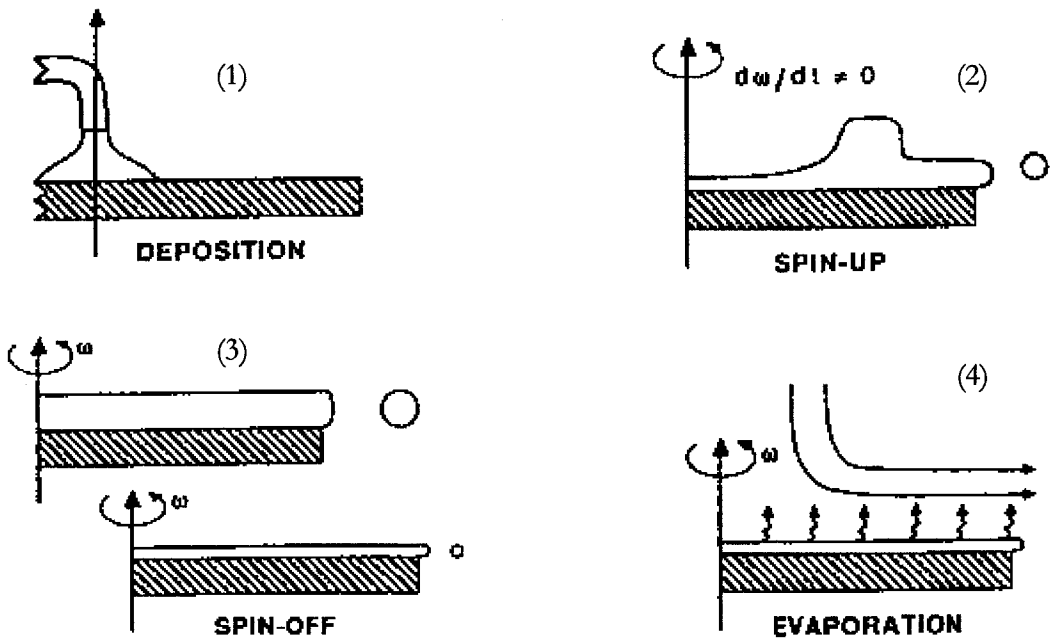


Figure 3-1 Stages of spin-coating process: (1) fluid dispensing; (2) acceleration; (3) constant-rate spinning characterized by gradual fluid thinning; (4) evaporation-dominated spinning [77].

The third stage is when the substrate is spinning at a constant rate and fluid viscous forces dominate fluid thinning behavior. This stage is characterized by gradual fluid thinning.

The fourth stage is when the substrate is spinning at a constant rate and solvent evaporation dominates the thinning behavior of the coated layer. As the prior stage advances, the fluid thickness reaches a point where the viscosity effects yield only rather minor net fluid flow. At this point, the evaporation of any volatile solvent species will become the dominant process occurring in the coating. In fact, at this point the coating effectively "gels" because as solvents are removed, the viscosity of the remaining solution will likely increase, effectively freezing the coating in place. This behavior was used in the seminal work of Meyerhofer [78] in which he quantified the coating thickness dependence on spin speed and viscosity and its relationship to the evaporation rate.

Clearly the third and fourth stages describe two processes that must be occurring simultaneously throughout the entire process (viscous flow and evaporation). However, at an engineering level, the viscous flow effects dominate early on while the evaporation processes dominate later.

3.1.1.2 Film thickness prediction

The starting point for much of the spin coating modeling was published by Emslie, Bonner, and Peck [79]. Their seminal treatment is based on assuming that flow has reached a stable condition where the centrifugal and viscous forces are just in balance (this is also the basis for most other modeling work – note that this does not apply to the first stage of spin-up and excess solvent expulsion). When the centrifugal and viscous forces are in balance, the following equation must be satisfied:

$$-\eta \frac{\partial^2 v}{\partial z^2} = \rho \omega^2 r \tag{3-1}$$

where z and r define a cylindrical coordinate system aligned with the axis of substrate rotation, v is the fluid velocity in the radial direction (a function of depth), ρ is the fluid

density, ω is the rotation rate in radians per second, and η is the viscosity in poise. With appropriate flow and velocity boundary conditions, and considering a film that is initially uniform, the film thickness as a function of time, h(t), was found to be:

$$h = \frac{h_0}{\sqrt{1+4Kh_0^2 t}} \tag{3-2}$$

where h_0 is the film thickness at the starting time (but not physically meaningful because of the first stage of unstable solution expulsion at early time), and K is a system constant defined as:

$$K = \frac{\rho\omega^2}{3\eta} \tag{3-3}$$

These equations are strictly valid only when K is constant. However, for spin coating of sol-gel or other complex solutions this may not hold true during all stages of spinning. Both viscosity and density are expected to increase as evaporation progresses, so caution must be used when applying these equations. In their analysis, Emslie et al. [79] also showed that for early stages of fluid thinning (before evaporation becomes important), the thinning rate would be defined as:

$$\frac{dh}{dt} = -2Kh^3 \tag{3-4}$$

At longer times, solvent evaporation becomes an important contribution. Meyerhofer was the first to estimate the effect of this on final coating thickness [78]. A quite reasonable approximation is that evaporation is constant throughout the spinning stages, as long as the rotational speed is held constant. Therefore, he simply added a constant evaporation term to the equation above. So, the governing differential equation became:

$$\frac{dh}{dt} = -2Kh^3 - e \tag{3-5}$$

where "e" is the evaporation rate [ml/s/cm^2] and this is effectively the contribution to the interface velocity that is driven by the evaporation process alone.

Instead of solving this equation explicitly, Meyerhofer [78] assumed that early stages were *entirely* flow dominated, while later stages would be *entirely* evaporation dominated. He set the transition point at the condition where the evaporation rate and the viscous flow rate became equal. This can be thought of as the fluid-dynamical "set" point of the coating process. When these assumptions are made, the final coating thickness, h_f, is predicted to be:

$$h_f = c_0\left(\frac{e}{2(1-c_0)K}\right)^{1/3} \tag{3-6}$$

where c_0 is the concentration of solids in the solution. When the physically applicable dependence of the evaporation rate on spin-speed was factored in, this was successful in matching the regular exponents for the dependence of final film thickness on spin speed. Research has shown that the evaporation rate should be constant over the entire substrate and depend on rotation rate according to:

$$e = C\sqrt{\omega}$$

where the proportionality constant, C, must be determined for the specific experimental conditions. This square root dependence arises from the rate-limiting-step being diffusion through a vapor boundary layer above the spinning disk. It should be noted that this results when airflow above the spinning substrate is laminar.

3.1.1.3 Fluid flow complications

The flow behavior described above ignores several effects that are important for many coating solutions. As noted above, the evaporation step is critical in defining what the final coating thickness will be. But, evaporation occurs from the top surface, and only some of the solution components are volatile enough to evaporate to any substantial degree. Thus, there will necessarily be an enrichment of the non-volatile components in the surface layer of the coating solution during the spinning process. One of the key consequences is that this surface layer will very likely have a higher viscosity than the unmodified starting solution. With a higher viscosity, it will then impede the flow characteristics set out above, making it a difficult differential equation to solve directly. This surface layer may also have the secondary effects of reducing the evaporation rate. So both the evaporation and flow processes are coupled through the behavior of the "skin" that develops on the top of the outwardly flowing solution during spin coating.

Another important effect is that some solutions are not "Newtonian" in their viscosity/shear-rate relationships. Some solutions change viscosity depending on what shear rate is used, thus depending on the distance from the center, the shear rate will be different and thus the flow behavior. This can give radial thickness variation that varies rather smoothly in a radial sense, as pointed out by Britten and Thomas [80].

3.1.1.4 Applications and limitations of spin-coating

Spin-coating technique finds itself useful in a variety of fields for thin film deposition because of its relatively low cost, high throughput and film thickness repeatability. In particular, it is very suitable for polymer thin film deposition.

However, spin-coated films usually suffer from pin-holes. When the film is very thin and the atmosphere is not clean, and/or there are bubbles in the solution, this problem is even more serious. Spin-coating in cleanroom and minimizing bubbles in the solution are usual approaches to cope with this problem. Spin-coating multiple ultra-thin films, if possible, may also block some pin-holes.

3.1.2 Inkjet Printing Technique

3.1.2.1 Inkjet printers

An inkjet printer is any printer that places extremely small droplets of ink onto substrates like paper to create a pattern. Those droplets are usually produced by a transducer illustrated in Figure 3-2. The transducer can be either a thin film resistor (heater) or a piezoelectric driver.

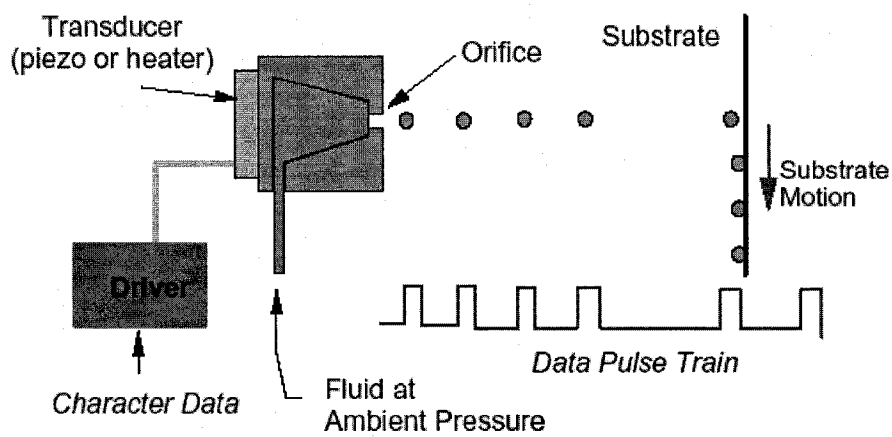


Figure 3-2 Schematic drawing element of an inkjet printer.

In the former case, a thin film resistor is fabricated on the inner wall of the ink cavity. When a high current is passed through the resistor, the ink in contact with it is vaporized, forming a vapor bubble over the resistor. The volumetric change by this vapor bubble causes pressure/velocity transients to occur in the fluid and produce a drop that

issues from an orifice. This type of printer is usually referred to as a thermal ink-jet printer.

In a piezoelectric inkjet system, a volumetric change in the fluid is induced by the application of a voltage pulse to a piezoelectric material that is coupled, directly or indirectly, to the fluid. Similarly, a drop is generated by the pressure due to the volumetric change. Figure 3-3 shows a piezoelectric inkjet printer that is used in our experiments.

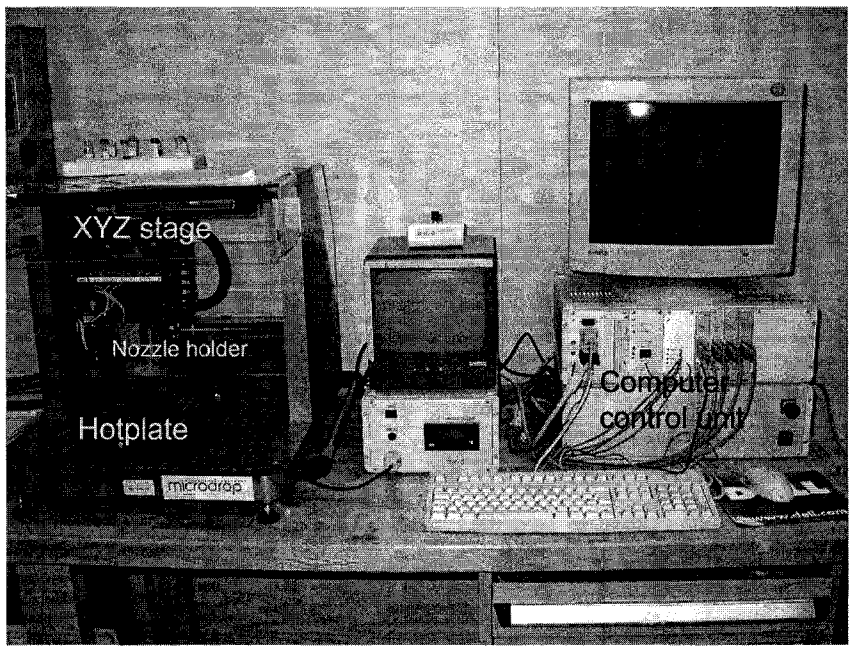


Figure 3-3 Microdrop dispensing system based on piezoelectric transducers.

It is a drop-on-demand Microdrop Dispensing System (Microdrop GmbH, Figure 1) interfaced with a computer. A piezoelectric nozzle together with a 4 ml ink reservoir is installed on the dispensing racket, which is capable of accommodating four nozzles simultaneously. The nozzle is activated by a voltage pulse, of which the voltage amplitude, pulse width, and frequency are adjustable through the computer software. A positioning system controls the movements of the nozzle in a XYZ station. The positioning accuracy is

±10 μm. The repetition accuracy is ±3 μm. The minimum step width of movement is 1 μm in X, Y and Z directions. The substrate stage is a hotplate controlled by a proportional, integral, and derivative regulator so that the substrate can be heated up to 150 °C.

3.1.2.2 Factors affecting inkjet printing

The general fluid property requirements for a fluid to be used in a piezoelectric drop-on-demand mode ink-jet device are as follows:

Viscosity: 0.5-40 centipoises; surface tension: 20-70 mN/m.

Some fluids with properties outside these ranges may be dispensed using ink-jet devices, but with increased difficulty and decreased performance. Combinations of the extreme values may also have poorer performance. If the fluid is heated or cooled, the above properties are required at the orifice.

Newtonian behavior is not strictly required, but the fluid properties at the orifice flow conditions must be in the above range. Thus, if the fluid has a low shear rate viscosity much higher than 40 centipoises, the viscoelastic behavior will cause significant performance problems.

Particle suspensions, such as inks, are acceptable as long as the particle or agglomerate size and density do not cause the suspension to depart from the fluid properties range given above. Particles that are >5% of the orifice diameter will cause at least some instability in drop generation behavior, but still may be acceptable in low concentrations.

The values above are appropriate for fluids with a specific gravity close to one. For high density fluids, such as molten metals, the values above should be converted to kinematical values using the density of water.

Increasing fluid viscosity acts to dampen the acoustic waves used to create a drop. Increasing viscosity also causes an increase in drive voltage required to create a drop of fixed velocity and a decrease in the effective orifice diameter, thus decreasing the drop size at fixed drop velocity.

Although surface tension and density are a weak function of temperature, viscosity is a strong function of temperature. Thus, the effect of viscosity variation can be shown most clearly by the operation of a fluid within a range of temperature.

Finally, viscosity acts to dampen the instabilities that lead to satellite droplets. Fluids with lower viscosity are more susceptible to satellite drop formation.

Surface tension has a small effect on the drive voltage requirements for a device. As surface tension increases, the drive voltage required to achieve a constant drop velocity will increase. Very low surface tension can result in an increased likelihood of air ingestion, particularly at high drop velocities. Very high surface tension materials require special consideration in the selection of orifice materials and coatings.

3.1.2.3 Applications and limitations of inkjet-printing

Historically, inkjet printing technique is widely used in the graphic arts printing world. Recently, this technique has been heavily explored for fabrication of polymer flexible electronic circuits due to its low cost, low temperature process, direct writing, solution processing and rapid prototyping [81]. Both organic and metallic components have been manufactured using this novel technique [82-85].

Unlike spin-coated films, the inkjet printed films are usually of poor uniformity. The film thickness variation may be as large as the film thickness value. Due to the coffee stain effect [86, 87], the inkjet printed dots may have ring-like structure, i.e., the film in the

rim region is over 10 times thicker than that in the center. This problem, however, can be solved by heating the substrate or using solvents with higher evaporation rate [86].

3.1.3 Self-Assembly Technique

3.1.3.1 Layer-by-layer self-assembly

Layer-by-layer (LbL) self-assembly is a novel method for film deposition in liquid (usually water) solution that makes use of the alternate adsorption of oppositely charged macromolecules (polymers, nanoparticles and proteins) [88-90]. The assembly of alternating layers of oppositely charged linear or branched polyions and nanoparticles is simple and provides the means to form 5 –500 nm thick films with monolayers of various substances growing in a pre-set sequence on any substrates at a growth step of about 1 nm. These films have a lower molecular order than Langmuir-Blodgett or free-standing films but they have the advantage of high strength and the easy preparation.

Figure 3-4 illustrates the basic principle and operation of LbL self-assembly. A cleaned substrate of any shape and dimension is immersed into a dilute solution of a cationic polyelectrolyte, for a time optimized for the adsorption of a single monolayer (ca. 1 nm thick), and then it is rinsed and dried. The next step is the immersion of the polycation-covered substrate into a dilute dispersion of polyanions or negatively charged nanoparticles also for a time optimized for the adsorption of a monolayer, and then it is rinsed and dried. These operations complete the self-assembly of a polyelectrolyte monolayer and monoparticulate layer sandwich unit onto the substrate. Subsequent sandwich units are self-assembled analogously. Linear polycation/polyanion multilayers can be assembled by similar means. Different nanoparticles, enzymes and polyions may be assembled in a pre-planned order in a single film.

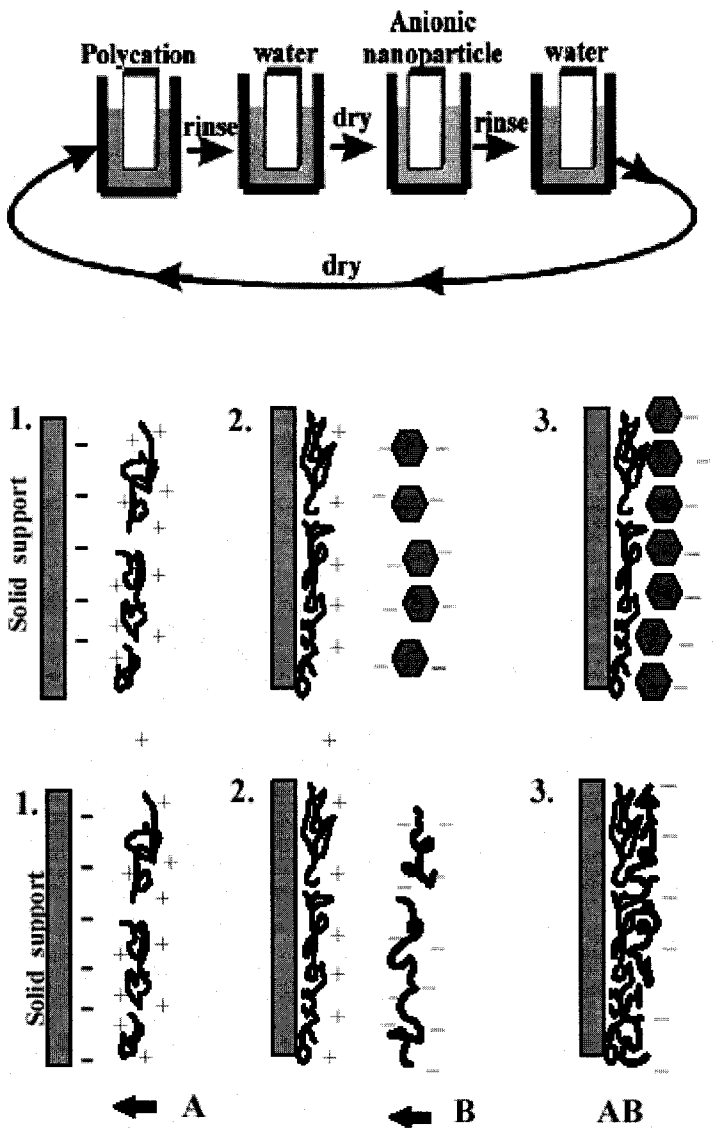


Figure 3-4 Schematic illustration of layer-by-layer self-assembly.

The forces between nanoparticles and binder layers govern the spontaneous layer-by-layer self-assembly of ultrathin films. These forces are primarily electrostatic and covalent in nature, but they can also involve hydrogen bonding, hydrophobic and other types of interactions. The properties of the self-assembled multilayers depend on the choice of building blocks used and their rational organization and integration along the axis perpendicular to the substrate.

3.1.3.2 Self-assembly monolayers

The formation of a well-packed monolayer from aqueous solution surfaces onto solid substrates was demonstrated a long time ago by the Langmuir-Blodgett (LB) technique [91]. LB-film formation is, however, cumbersome and time-consuming and requires a film balance. These problems have been overcome by the spontaneous formation of self-assembled monolayers (SAMs) on substrates [92, 93]. Self-assembly is governed by the strong attraction of an appropriately functionalized head group onto the substrate surface and by the hydrophobic interaction between the hydrocarbon tails of the molecules constituting the SAM. Formation of a SAM can be monitored, in situ, by electrochemical (quartz crystal microbalance, cyclic voltammetry, and impedance spectroscopy) and optical (ellipsometry [94], surface plasmon resonance imaging [95], and infrared reflection absorption spectroscopy [96]) measurements. The structure of the SAM formed can be imaged, ex situ, by microscopic techniques (scanning electron microscopy and scanning force microscopy).

Two different methods are practiced today for the spontaneous formation of SAMs on substrates. The first method involves the silanation of the substrate (typically glass) by surfactant silanes or siloxanes. Formation of sulfur coinage-metal (most often gold) covalent bonds represents the second method of SAM formation [97]. Both methods are attractive since they avoid the complex mechanical manipulation required for making LB films and since they are economical and suitable to scale up.

There is an additional important difference between LB films and SAMs. In LB film the configuration of the surfactants, determined by the parameters which are responsible for monolayer formation, is retained regardless of the type of substrate. In

contrast, in SAMs the surfactant organization is primarily dependent on the nature of the substrate.

Sagiv and co-workers first demonstrated a silane-based SAM on various substrates [98]. They immersed scrupulously clean glass, poly(vinyl alcohol), oxidized polyethylene, and evaporated aluminum substrates into millimolar solutions of n-octadecyltrichlorosilane (OTS) in an organic (80% n-hexadecane, 12% CCl_4, and 8% $CHCl_3$) solvent for a few minutes and obtained a well-packed SAM. The mechanism of self-assembly was discussed in terms of chemisorption and hydrolysis of the Si-Cl bonds at the substrate surface and subsequent formation of a network of Si-O-Si bonds (Figure 3-5).

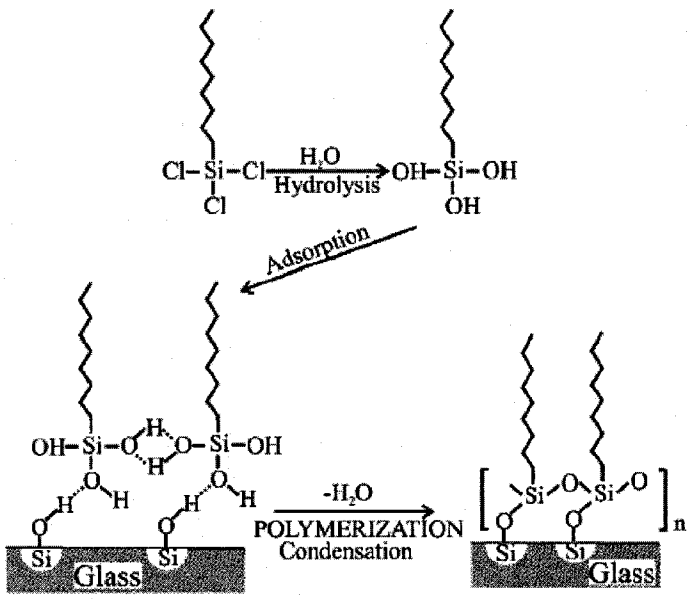


Figure 3-5 Schematic OTS SAM formation on a glass substrate.

Recent theoretical and experimental studies established the energy offsets between a silicon conduction band and the lowest unoccupied molecular orbital (LUMO) to be between 4.1 and 4.3 eV and that between the silicon valence band and the highest

occupied molecular orbital (HOMO) of the alkyl chains to be between 4.1 an 4.5 eV in siloxane SAM, irrespective of the alkyl chain length (between C12 and C18). These results validate the concept of using SAMs as ultrathin insulators. Preferential adsorption of silane surfactant molecules from a mixture depends on the structures of the amphiphiles and the substrate. Self-assembly by physisorption is reversible, while that of chemisorption is irreversible. Thus, surfactants physisorbed in monolayers can be replaced by surfactants which are able to chemisorb.

Both methods are promising for micro/nano-patterning [99]. On the other hand, they are also very useful for the stabilization and/or functionalization of metal nanoparticles (e.g., Au, Ag, Cu, Pd, and Pt) [100] and semiconductor quantum dots (e.g., CdSe, ZnS, and CdS) [101]. Figure 3-6 presents an example of surface capping by alkanethiol molecules.

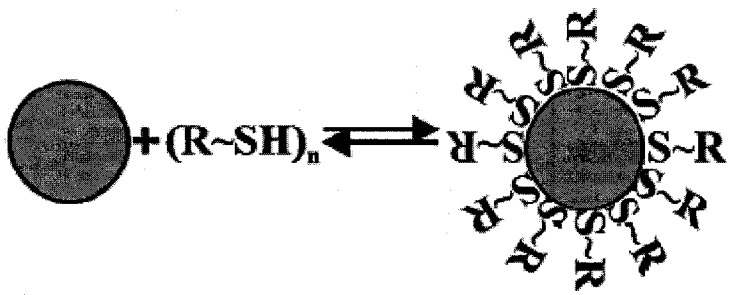


Figure 3-6 Schematics for surface capping of a nanoparticle by alkanethiol molecules.

3.1.4 Vacuum Thermal Evaporation

Thermal evaporation is a physical vapor deposition technique. It is conducted in the vacuum chamber of an evaporator (Figure 3-7). Basically, materials (for example, aluminum) are put in the tungsten filament bucket, which is then heated to the point

where the aluminum will actually evaporate. Aluminum vapor travels through the chamber and finally condenses in the form of a thin film on the (relatively) cold sample surface (as well as elsewhere in the chamber). The assembly of the technique is simple. It is appropriate for depositing metals and some compounds with low melting temperature (Al, Ag, Au, SiO, etc.). For materials with high melting point (W, Ta, Cr, C, etc) electron-beam evaporation is a good choice.

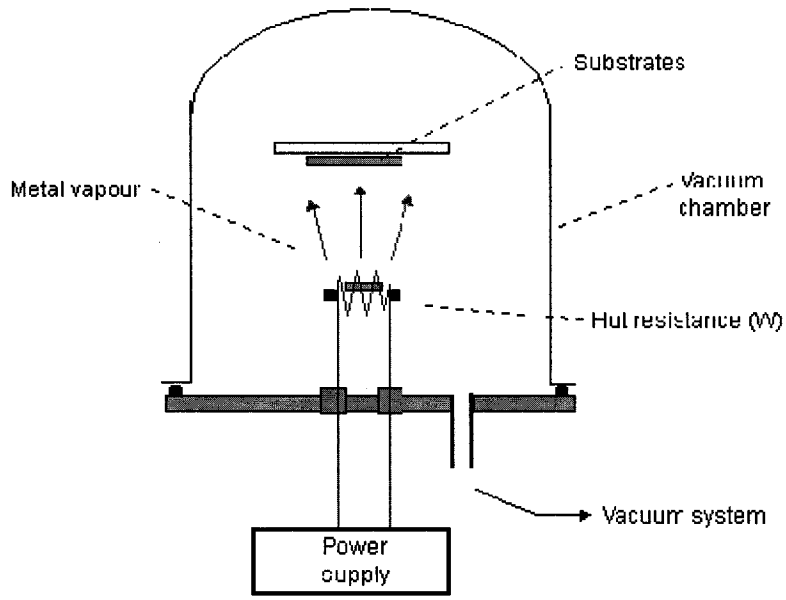


Figure 3-7 Schematics of vacuum thermal evaporation.

Usually low pressures, about 10^{-6} or 10^{-5} Torr, are used, to avoid reaction between the vapor and atmosphere. At these low pressures, the mean free path of vapor atoms is about the same order as the vacuum chamber dimensions, so these particles travel in straight lines from the evaporation source towards the substrate. This originates 'shadowing' phenomena with 3D objects, especially in those regions not directly accessible from the evaporation source (crucible). Besides, in thermal evaporation techniques the average energy of vapor atoms reaching the substrate surface is generally

low (on the order of kT, i.e. tenths of eV). This affects seriously the morphology of the films, often resulting in a porous and little adherent material.

3.2 Electrical Characterization Methods

All the fabricated devices need to be characterized for their current-voltage (I-V), capacitance-voltage (C-V) behavior, and sometimes current-time relationship. The basic equipment for these measurements is a computer-interfaced Keithley electrical characterization system (Figure 3-8). It consists of three I-V power sources and two C-V units. A probe station including four probes, a microscope and a CCD camera facilitates the testing of micro-scale devices. The voltage or current stimulus can be set up through the software, which also receives data and generates plots.

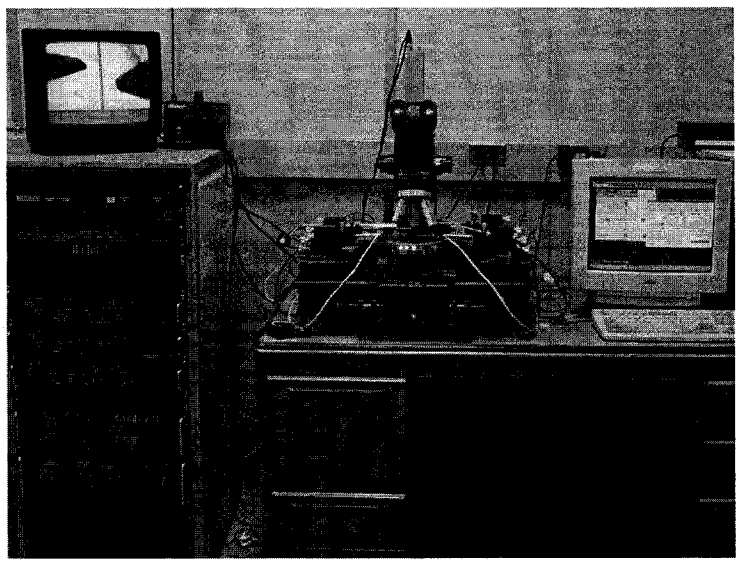


Figure 3-8 Keithley electrical characterization system.

CHAPTER FOUR

READ-ONLY ORGANIC RESISTIVE MEMORY DEVICE

4.1 Introduction

As mentioned in Chapter one, the charge-transfer complexes of TCNQ with metals or molecules show a wide range of interesting electronic properties. For example, Cu/TCNQ and C_{60}/TCNQ complexes can switch from 'low' conduction state to 'high' conduction state upon electrical bias, which enables them to be good candidates for data storage application.

Until now TCNQ-based complex thin films are either deposited in vacuum chamber [42, 43] or grown by immersing the substrate (e.g. Cu strip) in TCNQ solution [41, 102]. The former process is expensive while the latter one is not suitable for free-standing films. For low-cost applications, it is desirable to fabricate devices using solution-based processes like spin-coating. But TCNQ-based complexes are usually insoluble. In this work, we developed a soluble molecular complex composed of TCNQ and a methanofullerene derivative, namely [6,6]-phenyl C61-butyric acid methyl ester (PCBM). An electrically-bistable memory device was fabricated and characterized based on the spin-coated PCBM/TCNQ complex thin film.

4.2 Device Fabrication

The substrate is a glass slide, coated with a 200 nm thick aluminum by thermal evaporation method. The Al layer serves as the bottom electric contact.

PCBM molecules (structure shown in Figure 4-1a, purchased from American Dyes) were dissolved in chloroform at 6 mg/ml. The TCNQ solution in N,N-dimethylformamide (9 mg/ml) was added into PCBM solution according to the 1:1 molar ratio of PCBM/TCNQ. The mixture solution was magnetically stirred overnight. We found that the mixture solution of PCBM/TCNQ is very stable at room temperature. No precipitates were observed.

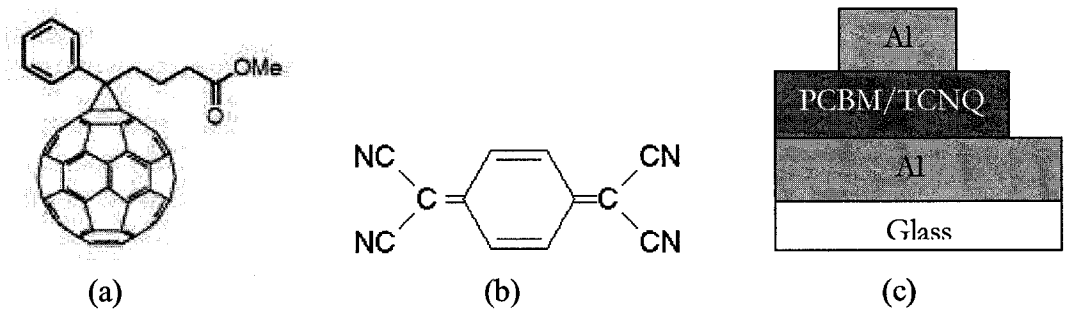


Figure 4-1 Schematic structure of PCBM (a), TCNQ (b), and the fabricated device(c).

The PCBM/TCNQ complex thin film was deposited by spin-coating the mixture solution over the aluminum-coated glass slide. The film thickness was measured to be ~100 nm on a Tencor Alpha step profilometer. Another aluminum layer was deposited on the organic thin film as the top electrodes by thermal evaporation through a shadow mask. A number of devices with Al-PCBM/TCNQ-Al sandwich structure (Figure 4-1c) were obtained. The active area of each device is 0.385 mm^2.

4.3 Experimental Results

UV-Visible absorbance spectra were obtained on an Agilent 8453 Absorbance Spectrometer. Both the PCBM/TCNQ chloroform solution in a quartz cuvette and the spin-coated PCBM/TCNQ film on fused quartz slide were characterized.

Figure 4-2 shows the UV-Visible absorbance spectra of the PCBM/TCNQ chloroform solution (upper) and spin-coated thin film (bottom). In chloroform solution, the co-presence of PCBM and TCNQ produces two new peaks (389 nm and 409 nm). As for the spin-coated film, the PCBM/TCNQ spectrum is not the linear combination of PCBM spectrum and TCNQ spectrum. We can see the shift of PCBM peaks toward longer wavelength. These results indicate the existence of the PCBM/TCNQ molecular complex.

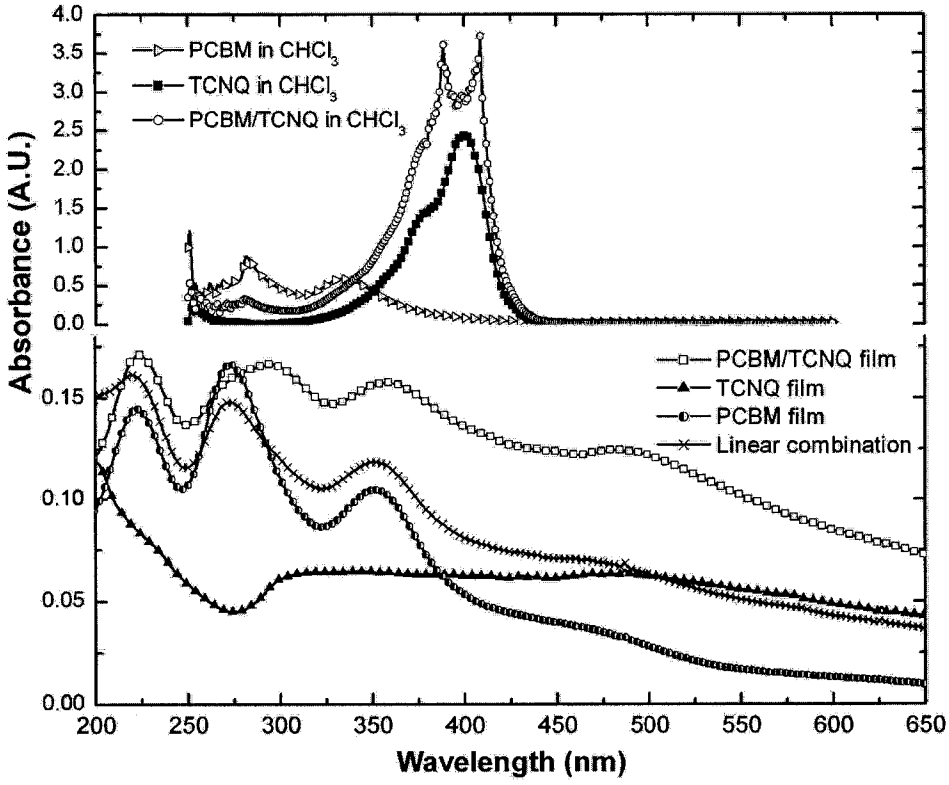


Figure 4-2 UV-Visible absorbance spectra of PCBM/TCNQ solution in chloroform (upper) and spin-cast thin film on fused quartz slides (bottom).

The spectrum of PCBM/TCNQ film is similar to that of PCBM. It seems that the absorbance of TCNQ, as well as the PCBM/TCNQ complex, is overwhelmed and/or suppressed in the solid film. This phenomenon can be attributed to the scattering of incident light beam by numerous tiny TCNQ crystals [103]. Owing to its much poorer solubility in chloroform, non-associated (or separated) TCNQ molecules crystallize much more effectively than PCBM. As a result, the dried film is probably a mixture of PCBM molecules, TCNQ crystals, and PCBM/TCNQ complexes. The optical images (Figure 4-3) of the films seem to support this description.

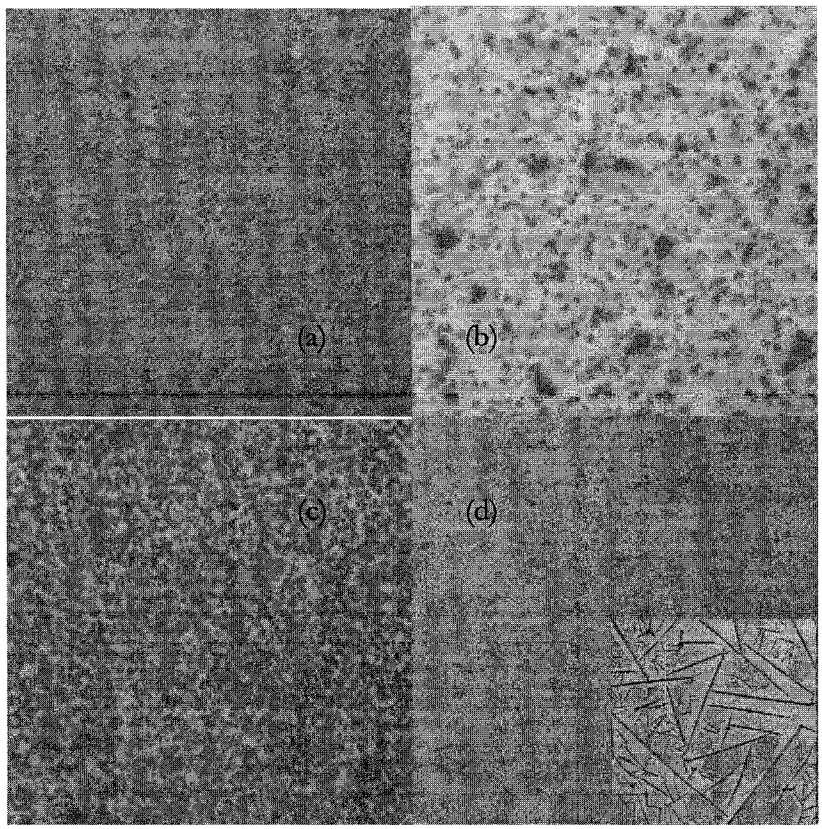


Figure 4-3 Optical images (1000 X) of the complex films with PCBM:TCNQ ratio of (a) 1:0, (b) 2:1, (c) 1:1, and (d) 0:1. Inset of (d) is 50X.

Figure 4-3 shows the surface morphology of the spin-coated thin films. It can be seen that there are black island structures embedded in the bulk film. The amount of black phase increases with the content of TCNQ. Therefore, we can identify the black phase as the TCNQ-rich structure, probably PCBM/TCNQ complex. The TCNQ film without PCBM, formed from the TCNQ in DMF, is not continuous (see inset of Figure 4-3d). The needle-like TCNQ crystal structures make the film very rough. SEM image also shows the island-like structure in the film (Figure 4-4).

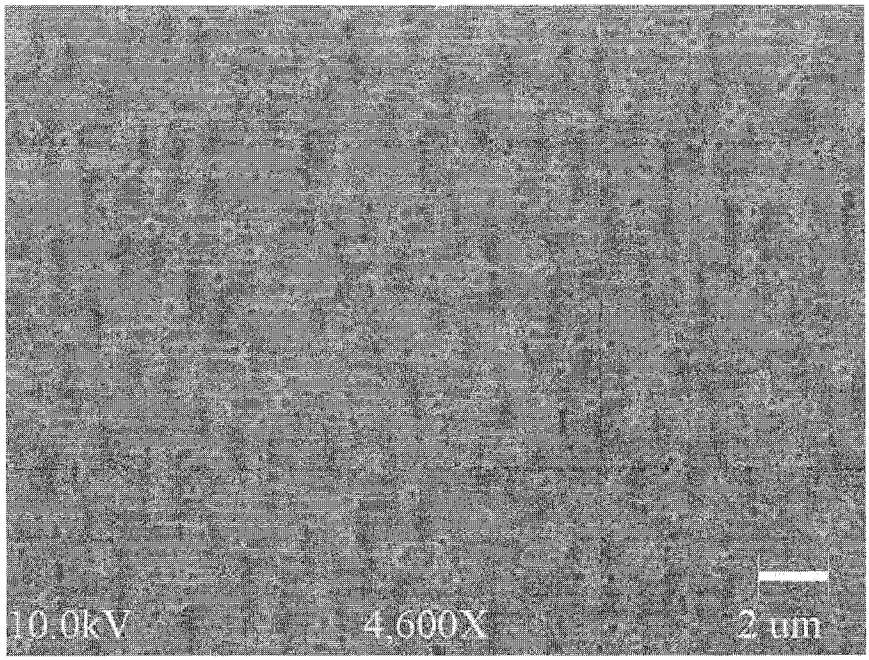


Figure 4-4 SEM image of the PCBM/TCNQ film.

All the devices were characterized using a electrical probe station with a computer-interfaced Keithley 236 power source. The current-voltage (I-V) characteristics of the Al-PCBM/TCNQ-Al devices are shown in Figure 4-5. It can be seen that the device switches from the initial low-conduction (or '0') state to a high-conduction (or '1') state at ~2.0 V. The on/off ratio is 1.76×10^{6} at 0.5 V, calculated from the data of curve I and curve II. Then

the device stays at '1' state even after the external electric field is removed. Figure 4-5 also shows the I-V curves of fresh devices versus the I-V curves of the same devices obtained after five months. It can be seen that either state of these devices remain stable in the air ambient. The change of ON-state current (at 0.5 V) is about -0.4%.

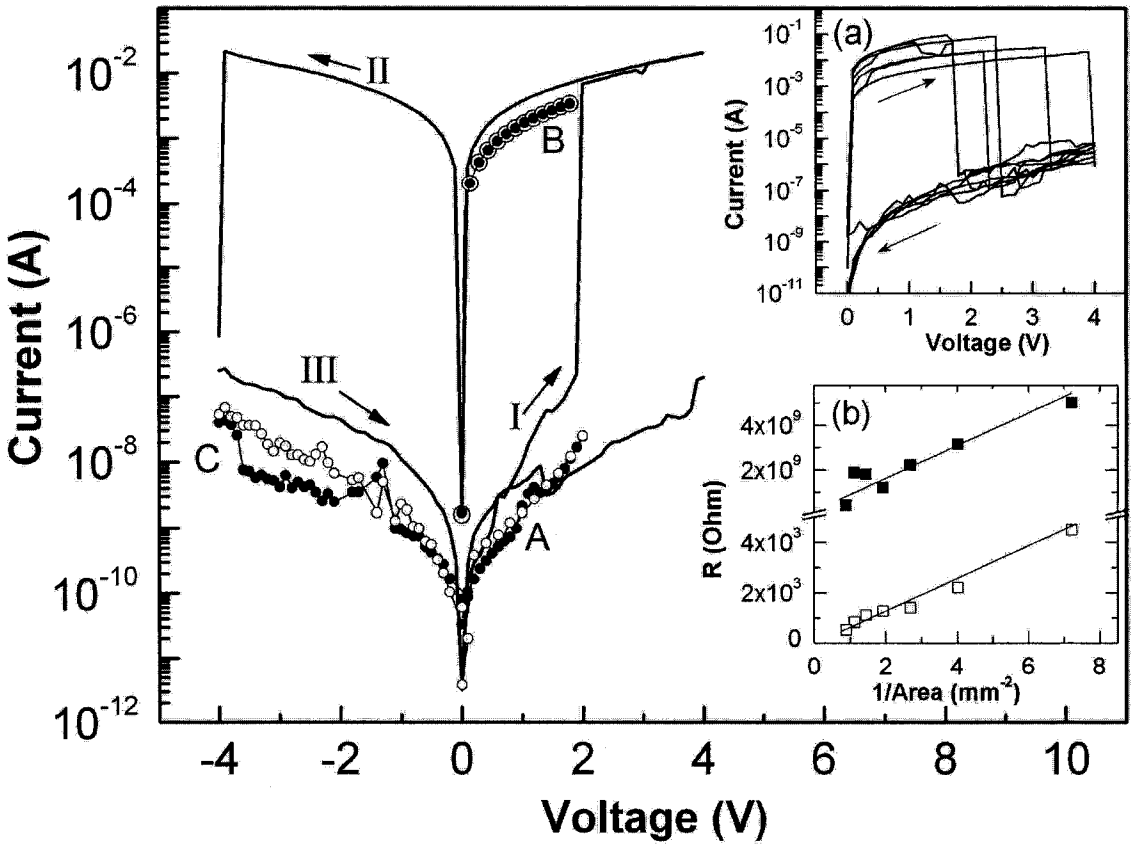


Figure 4-5 Current-voltage (I-V) characteristics of Al-PCBM/TCNQ-Al devices. The sequence of measurement is: curve I→ curve II→ curve III. I-V curves of three fresh devices (open circle) in initial OFF state (A), ON state (B) and 2nd OFF state (C), respectively, are also presented against the I-V curves of the same devices obtained five months later (solid circle). *Inset a*: switch-off of the programmed devices. *Inset b*: ON resistance (open square) and OFF resistance (solid square) versus 1/area. Each data point is the average value of six devices.

The device's conductivity abruptly drops down to its '0' level at -4.0 V. We believe it is the high current density that results in the switch-off. This is similar to Cu/CuTCNQ/Al

devices [41]. To verify the effect of high current density, a group of devices at '1' state were characterized. They all switch off when the current density reaches 5.0 to 25 A/cm^2. The inset *b* in Figure 4-4 shows the typical current-voltage characteristics of these programmed devices. The switch-off voltage varies from 1.5 V to 4.0 V. It should be mentioned that after switchback the devices do not switch to '1' state any more.

Devices of different areas (from 0.138 mm^2 to 1.108 mm^2) were fabricated and characterized. It is observed that the larger the device area is, the harder it is to switch off. However, quantitative comparison is difficult since the variation of switch-off current of same size devices is large (Figure 4-5 inset a). Large-area devices, e.g., > 0.7 mm^2, do not switch off even the current value reaches the limit (100 mA) of Keithley power source.

Considering the scalability, we calculated the nominal resistance (R) from the value of *V/I* at 0.5 V for both OFF state and ON state of devices with different active areas. The resistance versus area dependence is plotted as the inset b of Figure 4-5. Both the ON-state resistance and OFF-state resistance of these studied devices are roughly proportional to the reciprocal of device area. However, the scaling down of this device is obviously limited by the size (~1 μm) of film microstructures and by the film non-uniformity, as shown in Figure 4-3.

The yield of our devices is around 80%. This should be ascribed to the film non-uniformity, probably caused by TCNQ crystallization, and the pin holes, which are usually found in spin-coated films. Due to the same reasons the performance variation between devices is also large, as shown in Figure 4-5.

4.4 Discussion

4.4.1 I-V Curve Fits

To analyze the switching mechanism we plot the Log$I$-$V^{1/2}$ curve before switching (inset of Figure 4-5) and the Log$I$-Log$V$ curves after switchings (Figure 4-6). The linear Log$I$-$V^{1/2}$ relationship before the transition implies that the current is controlled by charge injection [104] from Al electrode into the PCBM/TCNQ molecular layer. After the first switching linear Log$I$-Log$V$ curves were obtained. The best linear fits of log$I$-log$V$ give $I \propto V^{1.1}$ for the 'ON' state and $I \propto V^{2.09}$ for the second 'OFF' state, respectively. At 'ON' state the current is basically ohmic. After switch-off it becomes space-charge-limited current, which requires at least one ohmic contact [105]. It seems that the electric switching changed the nature of the Al-organic contact from non-ohmic to ohmic.

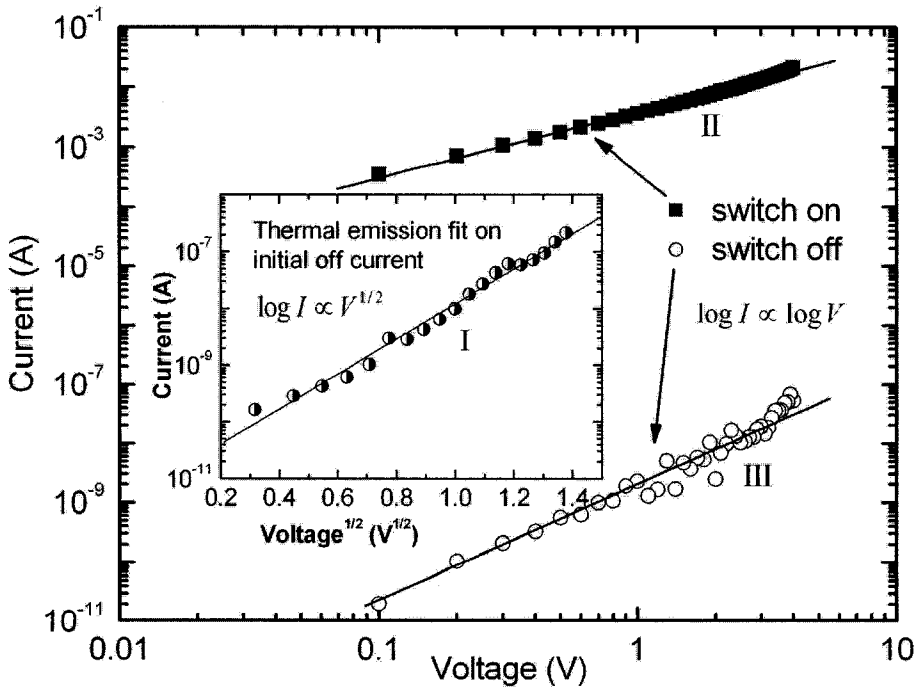


Figure 4-6 Current-voltage analysis of the device before switch-on (curve I of the inset), after switch-on (curve II) and after switch-off (curve III).

4.4.2 Effect of Film Composition

According to Oyamada et al. [42], no switching was observed of the TCNQ thin films. To further understand the switching and memory effect of PCBM/TCNQ films, we also studied the electrical behavior of Al-PCBM-Al devices, where the PCBM films were spin-cast from chloroform solution. As shown in Figure 4-7, bistable switching was observed in the device with PCBM film of ~100 nm thick. However, the device returns to low-conduction state when the voltage drops below 1.6~2.0 V. If the PCBM films are too thick (e.g., 200 nm) or too thin (e.g., 30 nm), there is no electrical switching.

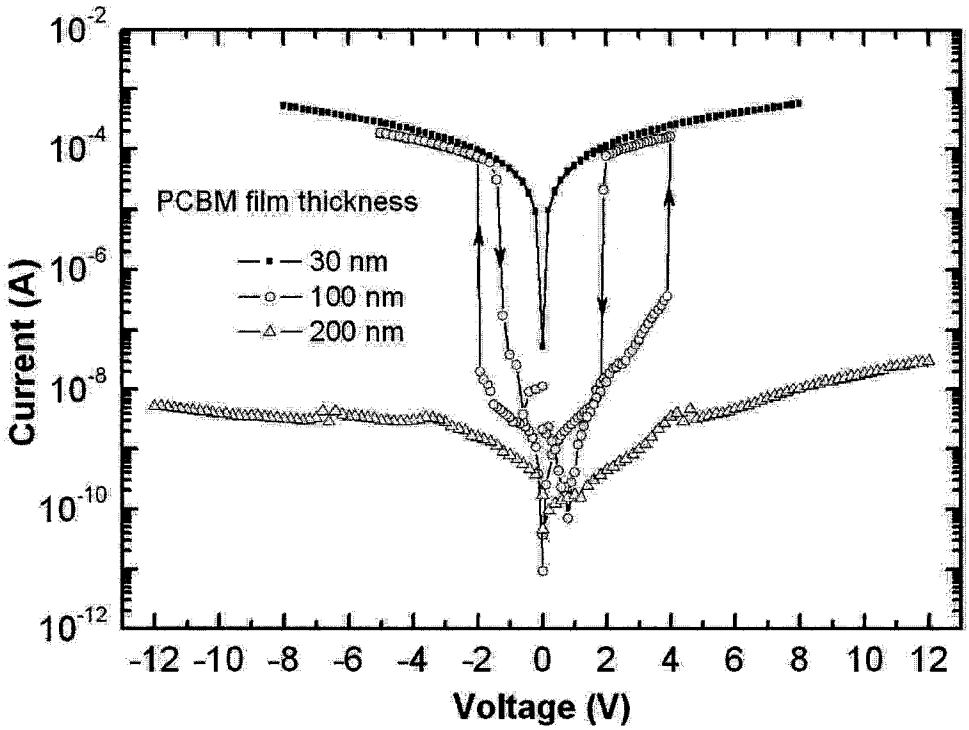


Figure 4-7 Current-voltage characteristics of Al-PCBM-Al devices with PCBM film thickness of 30 nm (solid square), 100 nm (open circle), and 200 nm (open triangle). Only the device with 100 nm PCBM film shows electrical switching.

Electrical bistability and memory effect were reported in Al-pentacene-Al structures [47]. Our Al-PCBM-Al devices are similar to them in terms of the dependence of

switching on the film thickness. It is well accepted that Al atoms can penetrate into the organic layer during the thermal evaporation. The electrical behavior of Al-PCBM (30 nm)-Al is probably caused by the penetration of Al through the PCBM film. If the molecular film thickness is appropriate, molecular quantum dot devices may form, as predicted by Alexandrov et al [106]. Their theoretical study shows that molecular quantum dots like fullerene derivatives exhibit electrical bistability in the voltage range $V_1 < V < V_2$, where V_2 is the switch-on voltage and V_1 is the switch-off voltage. According to Alexandrov et al [106], the thin native oxide on Al is desirable since the device requires weakly-coupled electric lead with the molecular quantum dots. The thin oxide is almost transparent for electrons while blocking the metal ion diffusion.

Comparing Figure 4-5 with Figure 4-7, we can see that the high-conduction state of PCBM/TCNQ device is non-volatile. PCBM has higher electron affinity (3.75 eV [107]) than TCNQ (2.8 eV [108]). In the PCBM/TCNQ complex it is reasonable to assume that some PCBM molecules (or clusters) are surrounded by TCNQ molecules. In this scenario the PCBM quantum dots become potential wells. Assuming that the quantum dot tunneling is still responsible for the switching, the charge trapping in the potential wells could be the reason of non-volatility. The electric field produced by trapped charge could work like the external electric field, keeping the device in the ON state. The trapped charge can also distort the band structure of surrounding molecular materials. Due to band distortion the energy barrier between the electrode and the molecules could become small and/or thin enough to result in ohmic-like behavior of the high-conduction state. High current density may heat some local places of the molecular film so as to damage the organic layer and switch the device off.

The role of TCNQ is further confirmed by the I-V curves of the devices with different PCBM/TCNQ molar ratios. Figure 4-8 presents the current-voltage curves of two devices with PCBM/TCNQ molar ratio 1:2 and 1:5, respectively. Both devices exhibit memory effects. It is expected that the more TCNQ present in the film, the higher switch-on voltage. But the device with PCBM/TCNQ = 1:5 has the switch-on voltage close to that of the 1:1 device (Figure 4-4). This is possibly caused by the higher degree of film non-uniformity due to the higher content of TCNQ molecules.

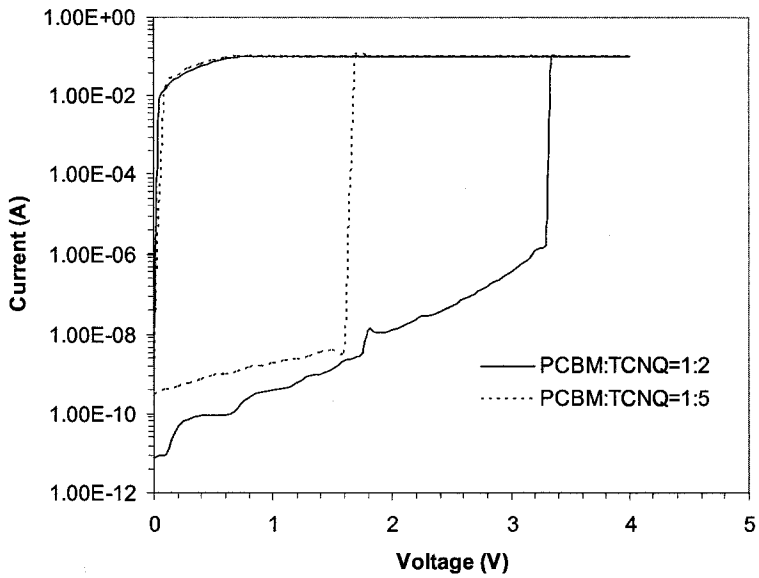


Figure 4-8 I-V curves of the Al-PCBM/TCNQ-Al devices with PCBM/TCNQ molar ratio of 1:2 (solid line) and 1:5 (dashed line), respectively.

4.4.3 Effect of Electrode Materials

To study the effect of electrode materials, indium tin oxide (ITO) instead of aluminum was used for the bottom electrode. Devices are showing similar switching behavior. However, the ON state disappears after the external electric field is removed (Figure 4-9). That means the device is volatile. Besides, the on/off ratio is also much smaller (1.28×10^3 at 0.5 V). The interesting thing is that the device becomes non-volatile

again when a conducting polymer PEDOT:PSS layer is inserted between the ITO contact and the molecular layer. The detailed experiments and mechanisms will be discussed in Chapter Five.

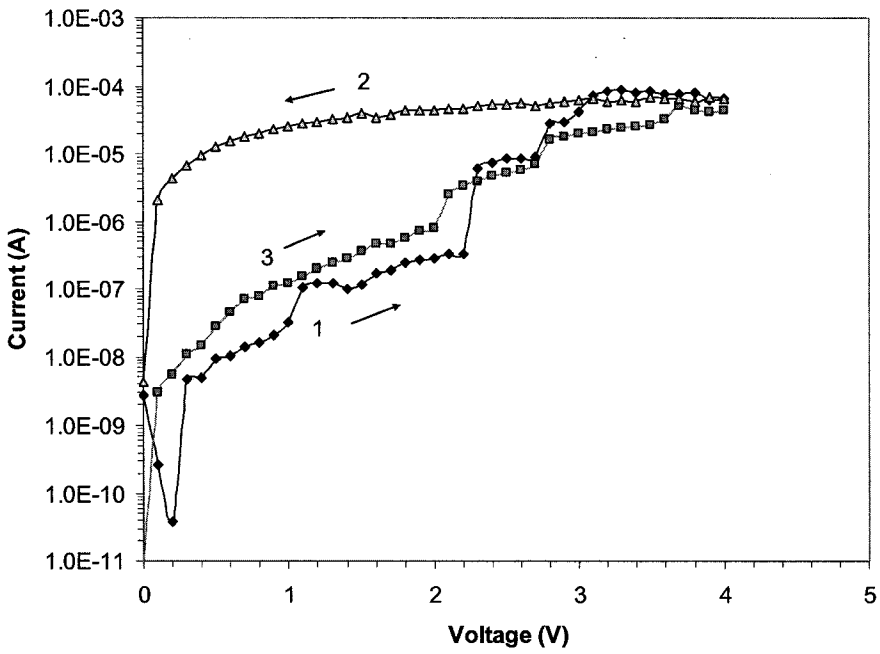


Figure 4-9 Current-voltage characteristics of the ITO-PCBM/TCNQ-Al devices. The number refers to the measurement sequence.

4.5 Summary

An organic electrically-bistable memory device based on the spin-coated molecular thin film has been demonstrated [109]. Sandwiched between two aluminum electrodes, the PCBM/TCNQ molecular film can switch from low-conduction state to high-conduction state, upon application of external electric field. A high current pulse can switch the device back to low conduction state. The device can remain at either state for at least five months after the external electric field is removed. This device is of potential use for low-cost write-once-read-many-times memory applications.

CHAPTER FIVE

REWRITABLE ORGANIC DIODE MEMORY DEVICE

5.1 Introduction

In Chapter Four, a read-only memory cell based on PCBM/TCNQ complex film is demonstrated. However, the device switches only twice. For wider applications it would be highly desirable to make the memory device rewritable. In this chapter, a rewritable memory device, in which PCBM/TCNQ complex film plays a role, will be presented. A theoretical model in terms of charge storage in the PCBM nanodots is proposed to explain the experimental results.

5.2 Device Fabrication and Characterization

The starting material is an ITO-coated (120 nm) PET transparency. First, the ITO transparency is cleaned by sonicating in acetone for 1 min and then in isopropyl alcohol for 10 min. Then the ITO surface is treated with O_2 plasma for 10 sec in order to obtain a hydrophilic surface and to increase the work function of ITO [110]. After that, a layer of conducting polymer poly(ethylene dioxythiophene): poly(styrene sulfonate) (PEDOT:PSS) is deposited on ITO by spin-coating method. The PEDOT:PSS layer is cured by heating the sample on a hotplate at 125 °C for 5 min. The thickness of PEDOT:PSS film is measured to be 200 nm. The PCBM/TCNQ (with a molar ratio 1:2) solution in a mixture of

chloroform and DMF is prepared as described in Chapter Four. The PCBM concentration is about 2 mg/ml. The mixture solution is spun on the PEDOT:PSS and then dried on a hotplate at 110 °C for one hour. The thickness of PCBM/TCNQ film is about 50 nm.

Finally, a 200 nm aluminum layer is deposited on top of PCBM/TCNQ film through a shadow mask. The active area is 0.385 mm^2. The final device has a structure schematically shown in Figure 5-1. Since PEDOT:PSS is a p-type material while both PCBM and TCNQ are n-type materials, a hetero p^+-N junction is expected to form between two organic layers. The device is some how similar to an OLED or organic solar cell. All devices are characterized using the Keithley electrical characterization system interfaced with a computer.

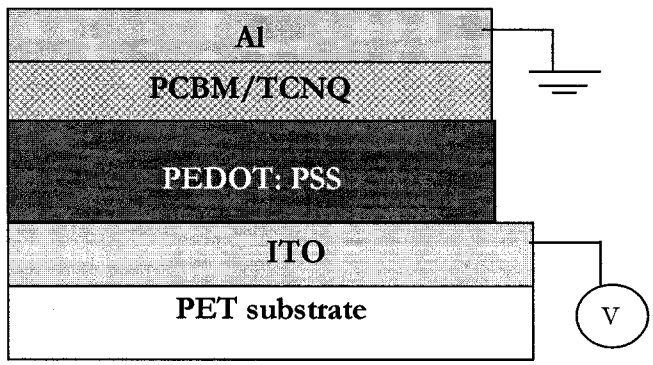


Figure 5-1 Schematic cross-section of the rewritable organic diode memory device.

5.3 Measurement Results and Discussion

The current-voltage characteristics of the device are shown in Figure 5-2. The curves exhibit repeatable hysteresis. When the voltage exceeds +5.0 V, the device switches to its ON state. Applying a negative voltage beyond -4.0 V switches the device off. The on/off ratio at +1.0 V is calculated to be 10^5. The switching can be repeated many times (>100).

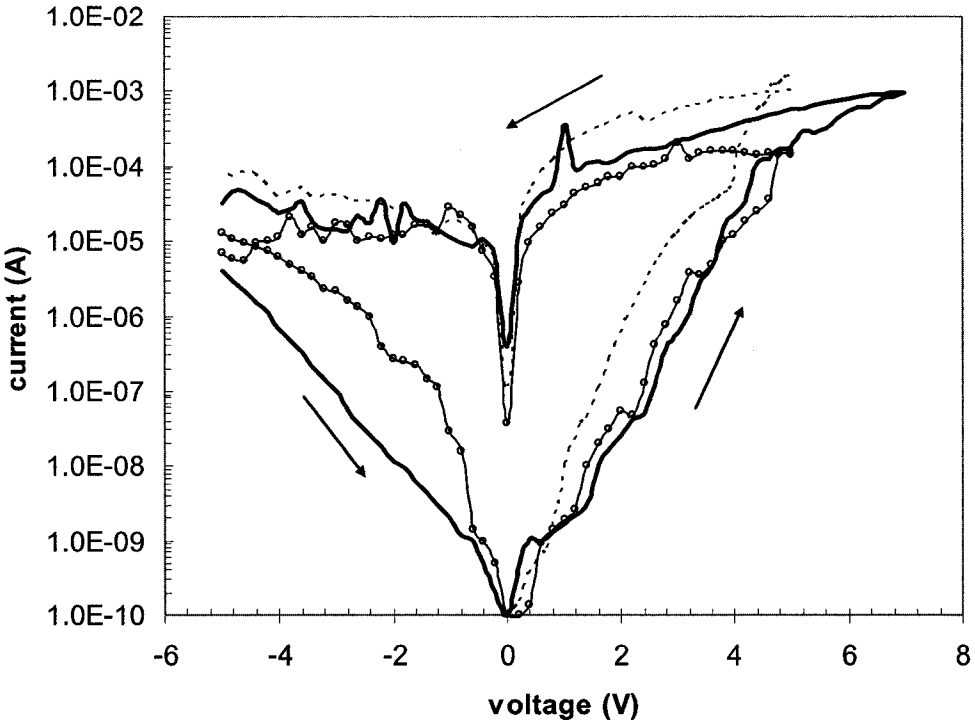


Figure 5-2 Current-voltage curves of the rewritable organic diode memory device.

The I-V curves in Figure 5-2 are not smooth, which may caused by two possible reasons. The first reason is the so-called Coulomb blockade effect [111], especially for the step-like features. In a tunnel junction the capacitance C is small enough that the energy associated with the transfer of one electron from a reservoir to the object is $E_c = e^2/2C$. When this energy is large compared with the available thermal energy, kT, and the tunnel resistance between the object and its surroundings R_T is much greater than the quantum resistance h/e^2, the transport properties of the system become strongly influenced by the discrete nature of the electron charge. The Coulomb blockage effect was observed as the steps of I-V curves, which also occurs in the low-conduction I-V curves of Figure 5-2. Those steps may be caused by the discrete charging and discharging of PCBM/TCNQ nanodots. The second reason is the noises, especially for those spikes of the I-V curves in

high-conduction state. For the p-n junction under forward bias, the total mean-square noise current (without considering 1/f noise) is given by [112]

$$\left\langle i_n^2 \right\rangle = 2qI_s Be^{\frac{qV}{kT}} - 2qBI_s, \tag{5-1}$$

where B is the band width and I_s the reverse bias saturation current. However, for the DC current measurement, the noise described in Equation (5-1) should be negligible. Therefore, the major noise here should be flicker noise or "1/f" noise because the integration parameter is set as 60 Hz in our I-V measurement. It was noted that the flicker noise was inversely proportional to frequency and consequently was predominant on the lower end of the frequency spectrum [113]. One physical origin is the poor contact between the probe and the device electrode. If the contact resistance changes due to the external reasons, for instance, the mechanical vibration of the probe station, the current level also change according to the diode current equation including resistance effect [114]:

$$I = I_s\left[\exp\left(\frac{qV - IR}{nkT}\right) - 1\right], \tag{5-2}$$

where R the parasitic resistance including contact resistance, n is the ideality factor.

It should be noted that the variation between different scan is relatively large. The reason is still not clear. The write-read-erase-read operations can still be realized, though. Figure 5-3a shows the cycles with write voltage +5.0 V, read voltage +1.0 V, and erase voltage -4.0 V. The current difference of over three orders of magnitude exists between the ON and OFF currents shown in solid circles (Figure 5-3b).

After the devices are programmed, as illustrated in Figure 5-3, the data retention is monitored using a probing voltage +1.0 V. Figure 5-4 shows the readout current versus time. We can see that both states are stable for over 10 minutes. However, both ON current

and OFF current decrease by two orders of magnitude after storing the device in air for two months. The possible reason is the degradation of organic materials, especially the degradation of PEDOT:PSS.

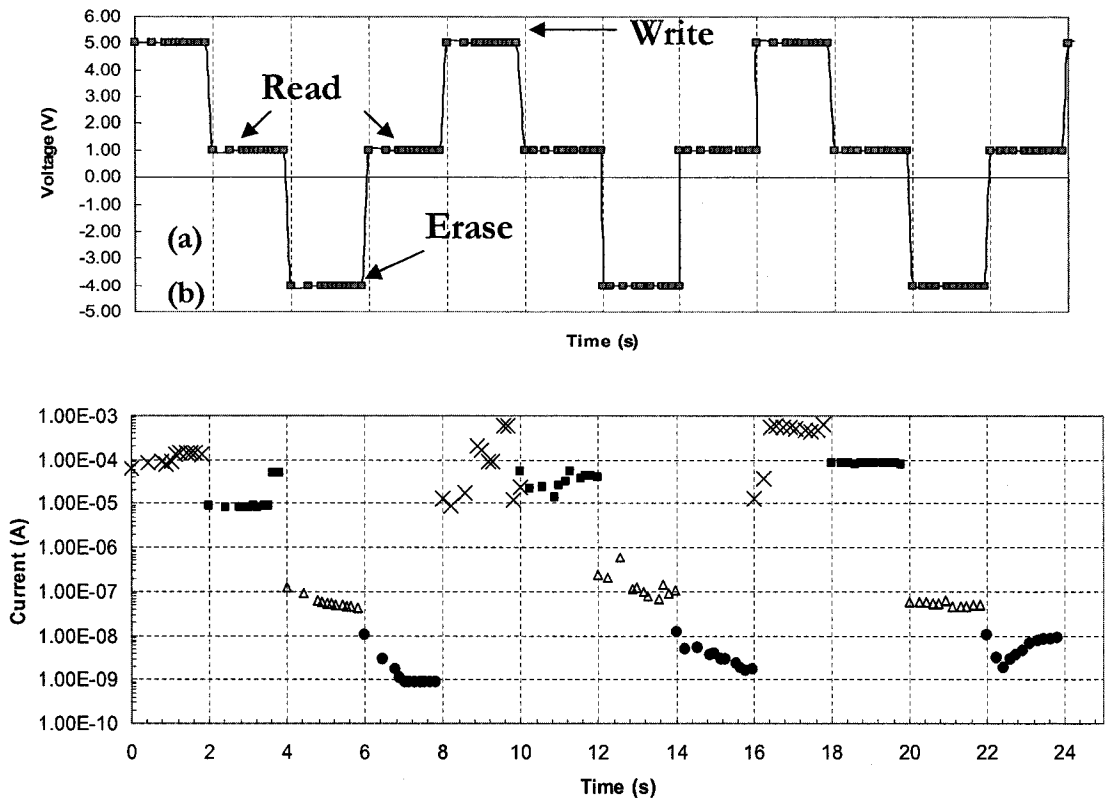


Figure 5-3 The write-read-erase-read cycles of the organic diode memory device.

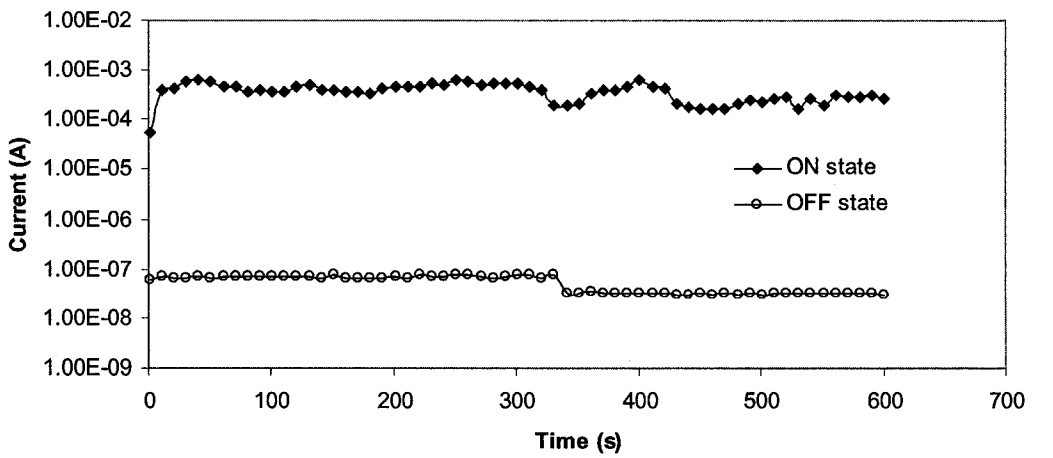


Figure 5-4 Data retention of the rewritable organic diode memory. The data were obtained by biasing the device at +1.0 V incessantly.

In order to understand the carrier transport mechanism in the device, the I-V curves of ON state and OFF state were studied using fitting methods. Figure 5-5a is the semilog I-V curve of OFF state, a linear LogI-V relationship can be found out, which implies a diode behavior of the device. It seems that the OFF current is mainly limited by the p^+-N heterojunction.

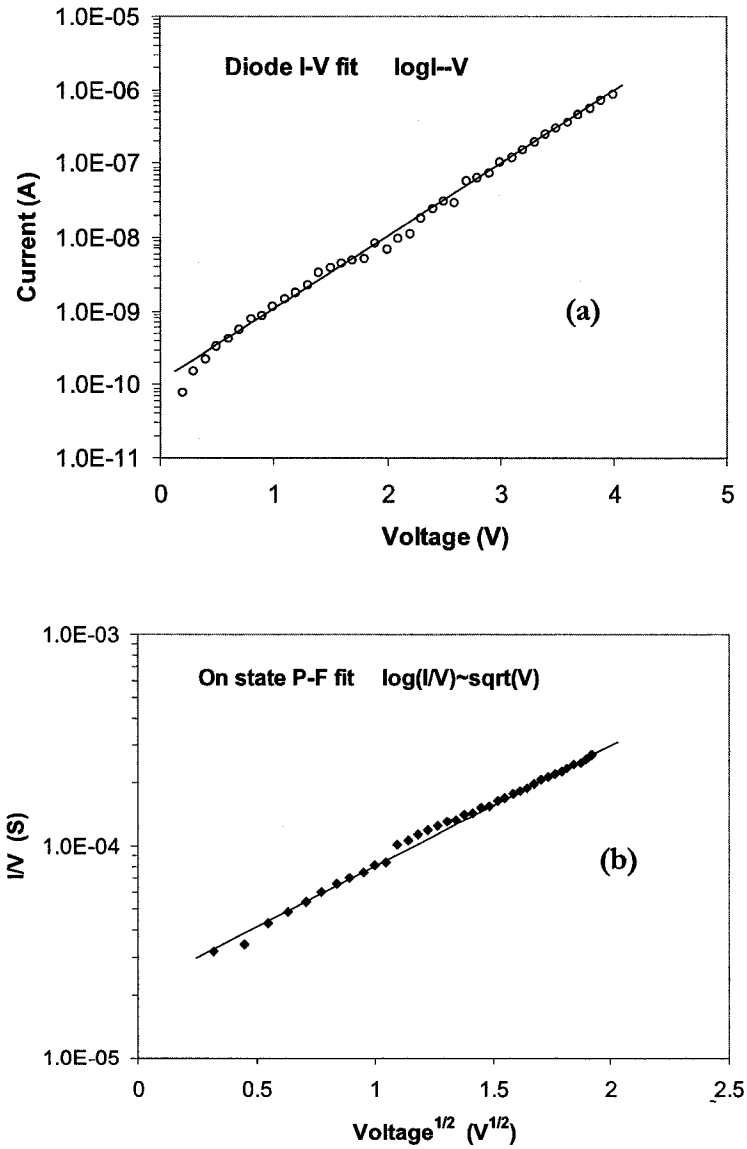


Figure 5-5 I-V curve analyses of the OFF state (a) and the ON state (b).

As for the ON state, the best fitting result gives the linear relationship $\log(I/V)$-$V^{1/2}$ (Figure 5-5b), which is the Poole-Frenkel (P-F) emission [115, 116]. P-F emission is featured by the structural defects causing additional energy states close to the band edge called traps. These traps restrict the current flow because of the capture and emission process, thereby becoming the dominant current mechanism. Therefore, from the I-V fit analyses, we can conclude that the current changed from a p^+-N heterojunction-limited mechanism in the OFF state to a charge capture-emission mechanism in the ON state.

To further understand this transition, the capacitance-voltage (C-V) characteristics of the device were obtained and plotted in Figure 5-6. The arrows show the direction of voltage scan.

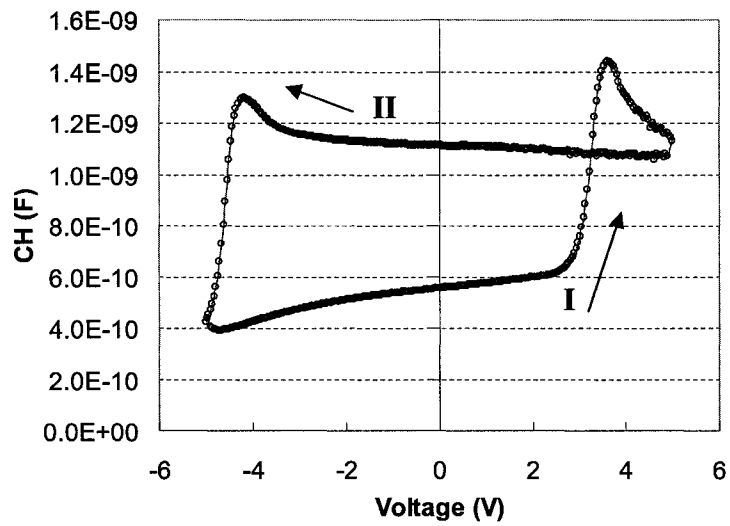


Figure 5-6 Capacitance-voltage characteristics of the ITO-PEDOT:PSS-PCBM/TCNQ-Al device at frequency100 kHz.

For a p^+-N heterojunction diode, the junction capacitance dominates in the reverse bias regime. Assuming $N_d << N_a$ and ϵ_p is close to ϵ_N, we have [112]

$$C_j = A\left[\frac{qN_dN_a\varepsilon_p\varepsilon_N}{2(\varepsilon_pN_a+\varepsilon_NN_d)(V_{bi}-V)}\right]^{1/2} \approx A\left[\frac{q\varepsilon_N}{2(V_{bi}-V)}N_d\right]^{1/2} \quad (5\text{-}3)$$

where A is the device area, V_{bi} is the built-in potential, ϵ_p and ϵ_N are the dielectric constants of p^+ region and N region, respectively, N_a and N_d are the acceptor concentration and donor concentration in the p^+ region and the N region, respectively.

Considering

$$x_N = \left[\frac{2N_a\varepsilon_p\varepsilon_N(V_{bi}-V)}{qN_d(\varepsilon_NN_d+\varepsilon_pN_a)}\right]^{1/2} \approx \left[\frac{2\varepsilon_N(V_{bi}-V)}{qN_d}\right]^{1/2}, \quad (5\text{-}4)$$

we can write Eqation (5-3) as

$$C_j \approx A\left[\frac{q\varepsilon_N}{2(V_{bi}-V)}N_d\right]^{1/2} = \frac{\varepsilon_NA}{x_N}. \quad (5\text{-}5)$$

In our p^+-N diode, the junction capacitance before charge storage (curve I in Figure 5-6) changes only slightly in the bias range from -5.0 V to +2.0 V. This result verifies the assumption that the N-region is completely depleted—depletion width x_N equals to the thickness of N-region d—even at positive bias.

In a p-n homojunction diode, the diffusion capacitance dominates in the forward bias regime. It can be described as [1, 112]

$$C_d = A\frac{q^2}{kT}\left(\frac{L_pp_n}{2}+\frac{L_nn_p}{2}\right)e^{\frac{qV}{kT}}. \quad (5\text{-}6)$$

where L_p (L_n) is the hole (electron) diffusion length, p_n (n_p) is the minority hole (electron) carrier density.

However, in our device the increase of diffusion capacitance with the direct current level ($\sim e^{\frac{qV}{kT}}$) is not observed. According to Sheinman and Ritter [117], the

diffusion capacitance should be omitted from the equivalent circuit of a p^+-N heterojunction diode, since the minority carriers in a abrupt p^+-N heterojunction do not contribute to the charging time of the diode due to the thermionic emission boundary condition.

At low forward bias, less than +2.0 V in our case, the differential charge appears at the edge of the depletion region, as expected in the depletion approximation. The junction capacitance roughly obeys the Equation (5-3), where x_N hardly changes.

Under high forward bias, the dopants near the junction are flooded by mobile carriers, the space charge region disappears, and the depletion charge should approach zero. The depletion capacitance should thus peak and then fall with increasing forward bias. For a high forward bias level, the capacitance can be expressed as [118]

$$C_j^{hi} = \frac{C_0}{\left(1-\frac{V_L}{V_B}\right)^M}\frac{dV_L}{dV}, \tag{5-7}$$

where C_0, V_B, and M are constants that depend on the heterojunction structure, $V_L(V) = R \cdot V_B - \frac{1}{G}\ln\left(1+e^{-G(V-R\cdot V_B)}\right)$ and R and G are adjustable constants.

The curve II in Figure 5-6 did not follow the track of curve I. The capacitance stays high when the voltage sweeps from +4.0 V to -4.0 V. This implies that the dopant ions near the junction are still flooded by charge carriers, and these charge carriers do not go away until a high negative voltage, say -5.0 V, is applied. Therefore, we can conclude that the charge is stored in the device after the forward bias.

Assuming that the dielectric constant of the organic films does not change, the amount of charge can be calculated from the C-V hysteresis loop according to the equation:

$$\Delta Q = \int_{V_1}^{V_2} (C_{forward} - C_{backward}) dV \tag{5-8}$$

where (V_1, V_2) is the voltage range, $C_{forward}$ and $C_{backward}$ corresponds to the capacitance values of forward scan and backward scan, respectively. To approximately calculate the charge ΔQ, equation (5-8) can be written as

$$\Delta Q = \sum_{i=0}^{n} [(C^{i}_{backward} - C^{i}_{forward})(V_{i+1} - V_i)] \tag{5-9}$$

where $V_0 = V_1$ and $V_n = V_2$ define the scan range.

The calculated ΔQ from the data of Figure 5-6 is 4.366×10^{-9} C for the device with area 0.385 mm^2. Therefore, the area charge density is 1.134×10^{-8} C/mm^2. This is equivalent to 7.09×10^{12} $electrons/cm^2$. If all the charge is uniformly trapped in the PCBM/TCNQ layer (~50 nm thick), then the volume charge density is 1.42×10^{18} cm^{-3}. If the charge is uniformly trapped in the whole organic layers, from PEDOT:PSS to PCBM/TCNQ, then the volume charge density is 2.83×10^{17} cm^{-3}. These values are relatively large as compared to the carrier density of PEDOT:PSS (1.17×10^{17} cm^{-3}), which we experimentally obtained from C-V and Hall effect measurements.

Based on the above I-V fit results and C-V measurement results, we can explain the electrical transition based on the charge storage model discussed in Chapter Two. The PEDOT:PSS/PCBM:TCNQ interface can be treated as a p^+-N heterojunction since the highly-conductive PEDOT:PSS is heavily-doped p-type semiconductor while PCBM and TCNQ are both n-type organic semiconductors with much wider band gaps (Figure 5-7). The transition from diode behavior to P-F regime implies the lowering of energy barrier across the p^+-N heterojunction.

We assume that in the organic molecular film some PCBM molecules (or nanocrystals) are surrounded by TCNQ molecules. In this scenario, just as mentioned in Chapter Four, a lot of nanosized potential wells (Figure 5-7a) are formed in the molecular complex film.

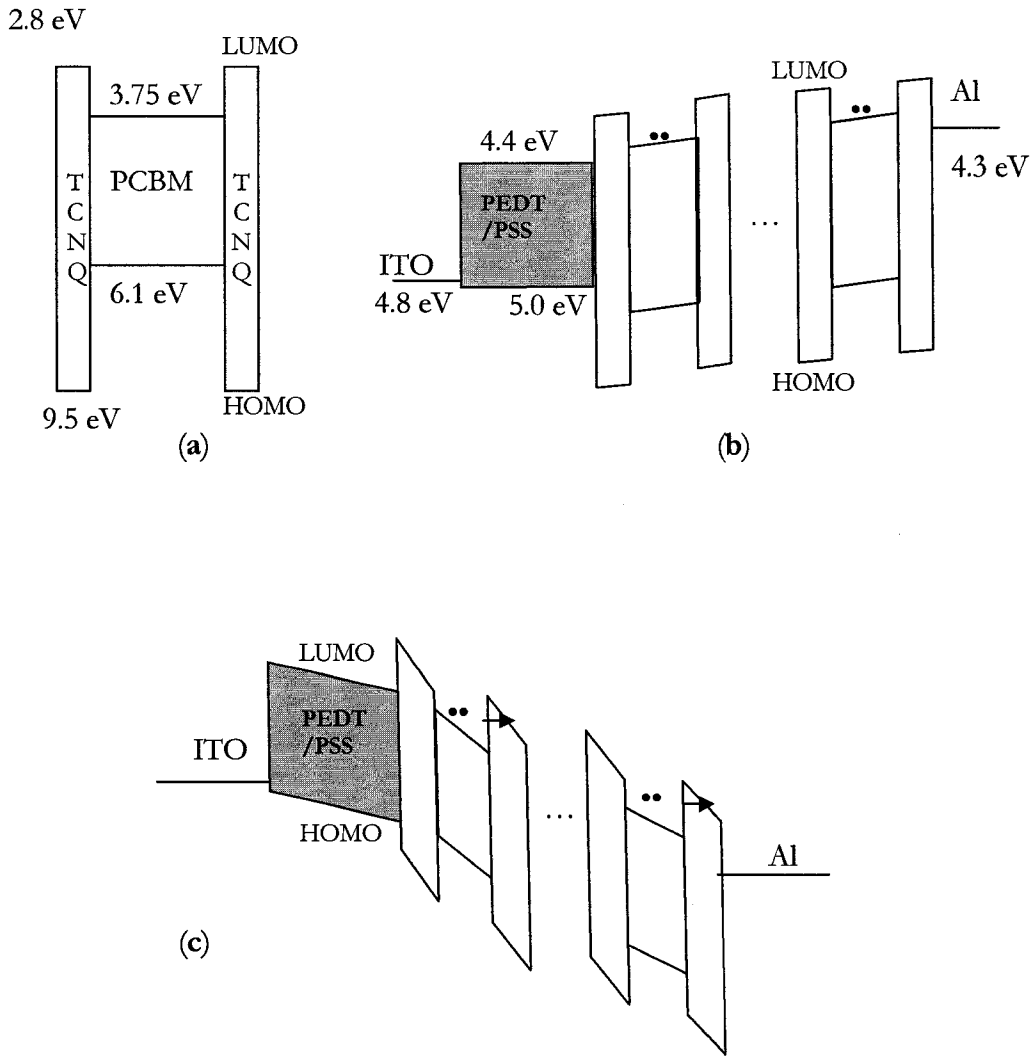


Figure 5-7 Proposed energy-band diagrams showing charge trapping mechanism in the film of PCBM/TCNQ. (a) Potential well formed by TCNQ wrapped PCBM; (b) Charge trapped in the potential wells; (c) Charge is driven out of the potential wells.

When the ITO electrode is positively biased, charge carriers flow across the p^+-N heterojunction. During this process, part of those charge carriers will be trapped in the potential wells, as well as in the defect traps. After the external voltage bias is removed, electrons (and/or holes) will be *still kept* in PCBM quantum dots surrounded by TCNQ molecules (Figure 5-7b). Trapped charge in the quantum dots produces electric field, which may (1) bend the band so as to lower the junction energy barrier and (2) change the conductivity of nearby semiconductor materials through the field effect. The lower barrier across the p^+-N heterjunction results in a P-F emission regime of the I-V characteristics.

When the ITO electrode is negatively biased, the charge stored in those energy wells will be driven out (Figure 5-7c). As a result, the device switches back to its injection-limited low-conduction state. The proposed model is consistent with the I-V and C-V experimental results.

5.4 Simulation Using Taurus-Medici

The effect of charge storage is also studied using TCAD tools Taurus. Detailed codes can be found in Appendix II. The simulations have been carried out for the p^+-N heterojunction diode by solving Poisson's equation and the hole and electron continuity equations with the program Taurus-Device [119]. All the tunneling models, including direct tunneling, F-N tunneling, and recombination by tunneling, are explicitly turned on.

Cathode and anode work functions are 4.3 eV (Al) and 4.7 eV (ITO) [74], respectively. Typical parameters of the organic layers are: For PEDOT:PSS, electron affinity $\chi = 3.9$ eV, band gap $E_g = 1.5$ eV, mobilities $\mu_p = 1.0\ cm^2 \cdot V^{-1} \cdot s^{-1}$, $\mu_n = 1\times10^{-7}\ cm^2 \cdot V^{-1} \cdot s^{-1}$ [49], N_c and N_v are estimated to be $10^{21}\ cm^{-3}$, active acceptor concentration $N_a = 1.2\times10^{17}\ cm^{-3}$ was obtained from C-V and Hall effect experiments. For PCBM, electron

affinity χ = 3.7 eV, band gap E_g = 2.4 eV, mobilities μ_p= 0.001 $cm^2 \cdot V^{-1} \cdot s^{-1}$, μ_n=0.002 $cm^2 \cdot V^{-1} \cdot s^{-1}$, $N_c=N_v=2.5\times10^{21}$ cm^{-3}, active donor concentration $N_d = 1.0\times10^{16}$ cm^{-3} [120]. For TCNQ, electron affinity χ= 2.8 eV, band gap Eg = 6.7 eV [108], mobilities μ_p=0.002 $cm^2 \cdot V^{-1} \cdot s^{-1}$, μ_n=0.003 $cm^2 \cdot V^{-1} \cdot s^{-1}$, $N_c=N_v=10^{21}$ cm^{-3}, active acceptor concentration N_d = 1.0×10^{15} cm^{-3} [121].

The simulated device structure, as shown in Figure 5-8b, is generated using Taurus-Process [122]. Nine TCNQ-wrapped PCBM nanodots are placed in the bulk PCBM layer (50 nm thick). Three floating gate contacts are defined enclosing the PCBM dots, which are required for placing charges onto the dot [119]. The thickness of PEDOT:PSS is 200 nm.

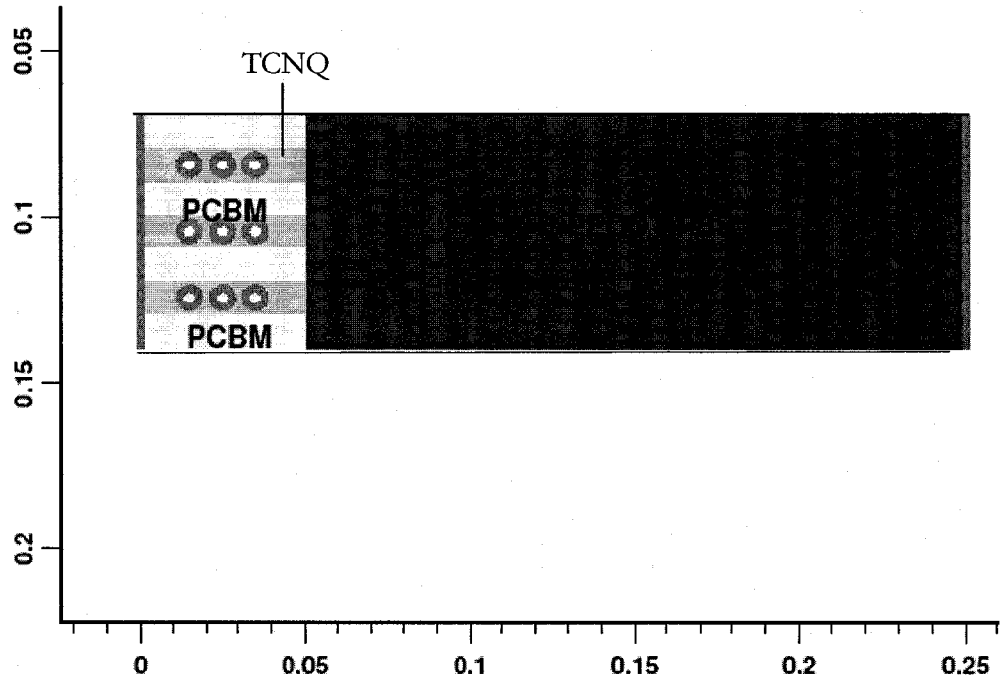


Figure 5-8 The simulated p^+-N diode device structure with nine PCBM nanodots.

From the C-V curves in Figure 5-6, the charge stored in the device is calculated to be 1.134×10^{-8} C/mm^2. The simulated device in Figure 5-8 has an area of 70 nm×1 μm = 7×10^{-8} mm^2. Hence, the charge amount $\Delta Q = (1.134\times10^{-8}) \times (7\times10^{-8}) = 7.938\times10^{-16}$ C is

intentionally placed on the nano-dots. The currents at low voltages are significantly increased due to the effect of introduced charge, as shown in Figure 5-9. The simulated on/off ratio at +0.5 V is 2.7×10^4, which is close to the experimental result, 3.5×10^4, calculated from the data shown in Figure 5-2. The shapes of the simulated I-V curves are also similar to the experimental I-V curves in Figure 5-2. But the simulated loop size is smaller. The deviation is probably caused by the omission of interfacial insulating layer PSS.

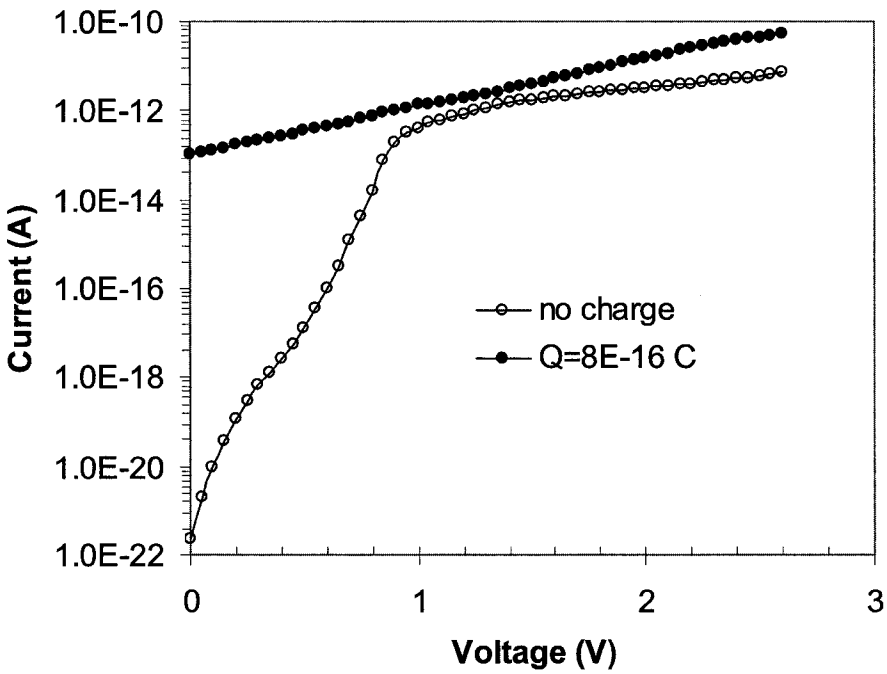


Figure 5-9 Simulated I-V curves of the above p^+-N diode.

5.5 Summary

A rewritable organic diode type memory device was realized based on the ITO/PEDOT:PSS/PCBM:TCNQ/Al structure. The device exhibits a diode characteristic (low conductive) before switching to a high-conductive P-F regime upon a positive external bias to ITO. The on/off ratio at +1.0 V is up to 10^5. After two months, the

resistances of both high-conduction and low-conduction states increase by a factor of two orders of magnitude. But the on/off ratio hardly changes, still ~10^5. A charge storage model is proposed to explain the memory effect. Simulation results from Taurus-Device are in qualitative agreement with the experimental results and the proposed model.

CHAPTER SIX

TRANSISTOR-TYPE ORGANIC MEMORY DEVICES

6.1 Introduction

To make a memory cell based on an organic field effect transistor (OFET) is an interesting option for organic memory. Until now it seems that all successful OFET memory devices [53-55, 123-125] are fabricated using a ferroelectric (or ferroelectric-like) gate dielectric materials, especially ferroelectric polymers [54]. The direction of the polarization of the gate dielectric layer modulates the transistor's channel conductance.

Another way to make an OFET memory is to introduce charge traps, e.g., nanoparticles, into the gate dielectric. This approach has seen a dramatic progress in the field of silicon-based non-volatile memory [26, 30-32], where high temperature processes are typically involved. Kolliopoulou et al. [126] integrated the organic insulator and gold nanoparticles in silicon-based field effect transistor by chemical processes and thus fabricated a hybrid transistor non-volatile memory at room temperature. Their work paved the way toward organic transistor memories.

In this chapter, an OFET memory with self-assembled gold nanoparticles as charge traps will be presented. The device is fabricated using low-temperature solution-

processing techniques, which are compatible with the usual plastic substrate such as poly (ethylene terephthalate) (PET), poly(ethylene naphthalate) (PEN) and polyimide. Therefore, the results of this study could accelerate achievement of cheap, fast and flexible organic non-volatile memories.

6.2 Modeling and Simulation of OFET Memory

The nanodot OFET memory devices are studied using TCAD tools Taurus-Tsuprem4 and Taurus-Medici. To reduce the computational load, the device structure is dramatically simplified (Figure 6-1). Au nanodots are treated as squares with side length of 20 nm.

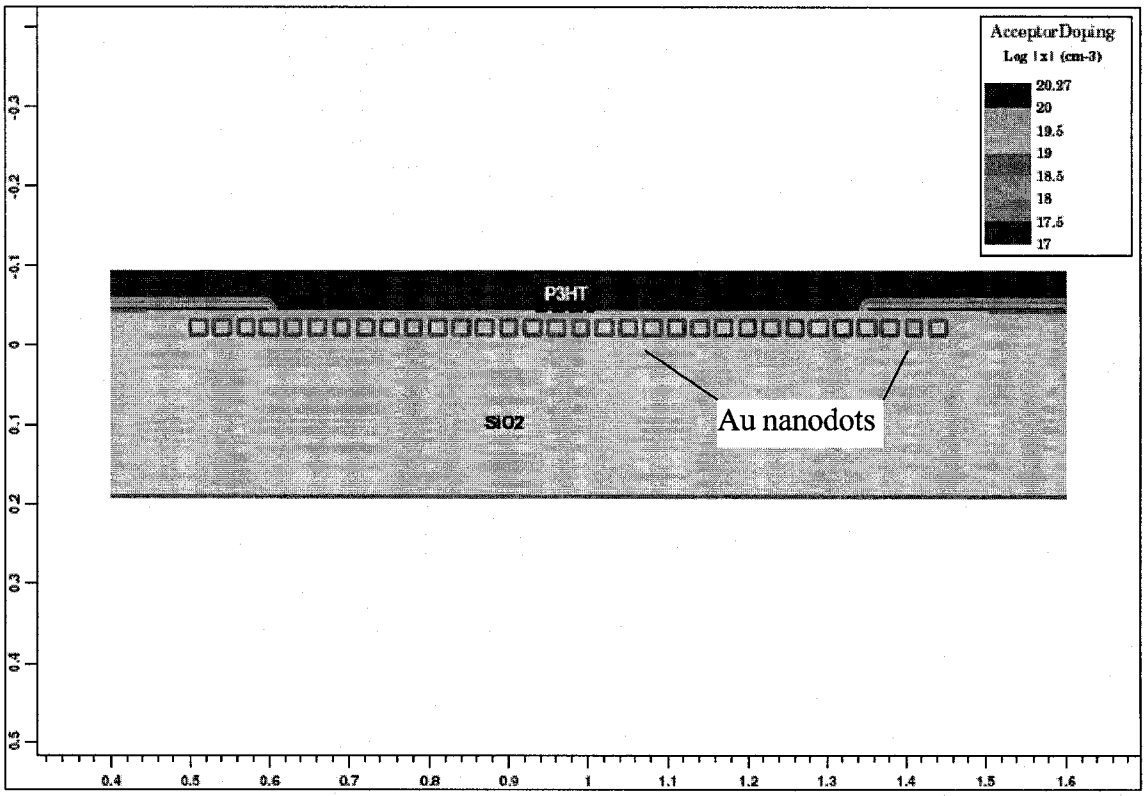


Figure 6-1 The simulated 2D device structure of the OFET memory cell

The channel material P3HT, a semiconductor polymer, is treated as Si with modified properties (bandgap, mobility, carrier concentration, dielectric constant etc). Here, electron affinity $\chi = 2.7$ eV, band gap $E_g = 2.2$ eV [127], mobilities $\mu_p = 5.0\times10^{-3}$ $cm^2 \cdot V^{-1} \cdot s^{-1}$ [128], $\mu_n = 6\times10^{-4}$ $cm^2 \cdot V^{-1} \cdot s^{-1}$ [127], N_c and N_v are estimated to be 10^{20} cm^{-3}, and the active acceptor concentration $N_a = 1\times10^{17}$ cm^{-3} is obtained from C-V measurements.

The source and drain material PEDOT:PSS, a p-type conducting polymer, is treated as p^+-Si, since the work function of PEDOT:PSS is 5.1 eV, very close the work function of p^+-Si, The floating gate containing random gold nanoparticles is treated as a row of spherical nanosized dots (diameter = 16 nm). Control gate dielectric is 100 nm SiO_2, which is not presented in Figure 6-1 in order to see the gold nanoparticles. In real device, the tunneling barrier (~10 nm) is insulating polymers. Unfortunately, we do not have the data about the electronic structure of insulating polymers such as PVP, PAH and PSS. Here we approximately treated them as silicon nitride. The channel length is 1.2 μm, which is quite small compared to those parameters of the real device. Below is the detailed procedure of modeling and simulation:

(1) Construct a device structure model using Taurus-Tsuprem4;

(2) Using Taurus-Medici to simulate the transient process of charge storage and obtain the amount of charge during a fixed charging time;

(3) Set the amount of floating gate charge as the value obtained in step (2) and simulate the I_{ds}-V_{gs} characteristics of the OFET. Then compare the results with that of the device without floating gate charge.

The device structure is constructed using Taurus-Process. First, a row of spherical cavities were defined inside the oxide region; then the cavities were filled with metal

nickel, whose work function is adjusted to be gold's work function 5.1 eV in the 'physics' command. A definition of floating gate contact is required to simulate the charging and discharging of metal nanodots. If one region is wrapped by the floating gate contact, the Poisson's equation will be disabled in that region.

The charge boundary condition for the floating region, i.e., metal nanodots, is implemented. For each floating electrode specified, a value of the net charge is used in the boundary condition. This net charge is either specified (for steady state) or generated by the tunneling and injection models in transient analysis and automatically placed on the floating electrodes [119]. The charge boundary condition is specified as:

$$\oint \vec{D} \cdot d\vec{S} = Q, \tag{6-1}$$

where Q is the total charge on the floating electrode.

The net charge Q can be generated by transient simulation. By default, the hot carrier injection model and Fowler-Nordheim tunneling model are automatically turned on when transient simulation is performed with charge boundary condition. However, if the direct tunneling model is used in place of F-N tunneling, one needs to turn it on manually. During transient simulations, the incremental charge obtained from integrating the tunneling current over time is immediately placed on the appropriate electrodes [119].

From the transient simulations the data of stored charge amount versus time (Q-t) can be obtained, as shown in Figure 6-2. We can see that the gold nanoparticles do trap charges when the gate is negatively biased. The higher the V_{gs} is, the more the charge amount for a fixed charging time. In Figure 6-2, the effect of tunnel barrier thickness is also studied. As expected, the thinner the tunnel barrier is, the easier the gold nanodots are charged. The net charge on the floating gate is automatically generated to be -3.5×10^{-15} C,

given the program time 0.1 s. The I_{ds}-V_{gs} characteristics of the OFET is then simulated (Figure 6-3). V_T of the OFET shifts toward negative direction.

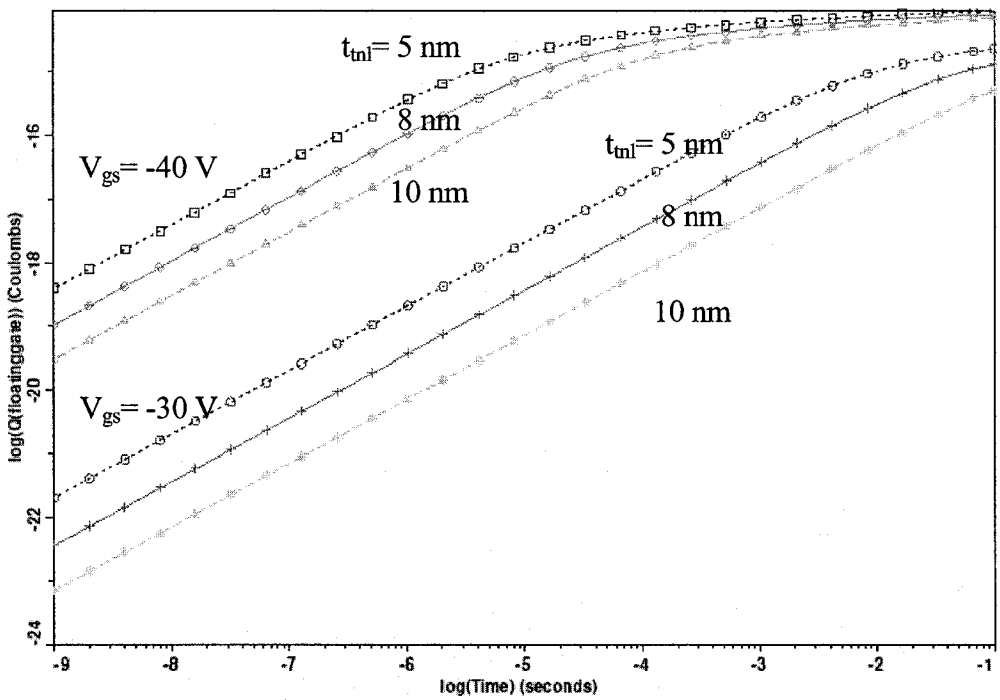


Figure 6-2 Simulated charging transient of the floating gate. V_{ds}=0 V.

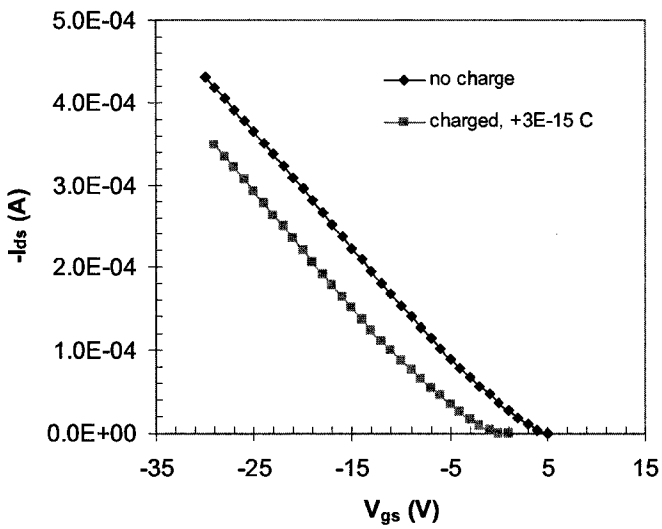


Figure 6-3 Simulated transfer characteristics of nanodot OFET memory. Negative V_T shift is observed when the floating gate is positively charged.

Sincere the metal nanodots are intrinsically 3D structures; 3D simulation is expected to give more accurate results. In order to compare the simulation results, a 3D device structure model (Figure 6-4) is also constructed with Taurus-Process according to the similar procedures described before. The program codes can be found in Appendix III.

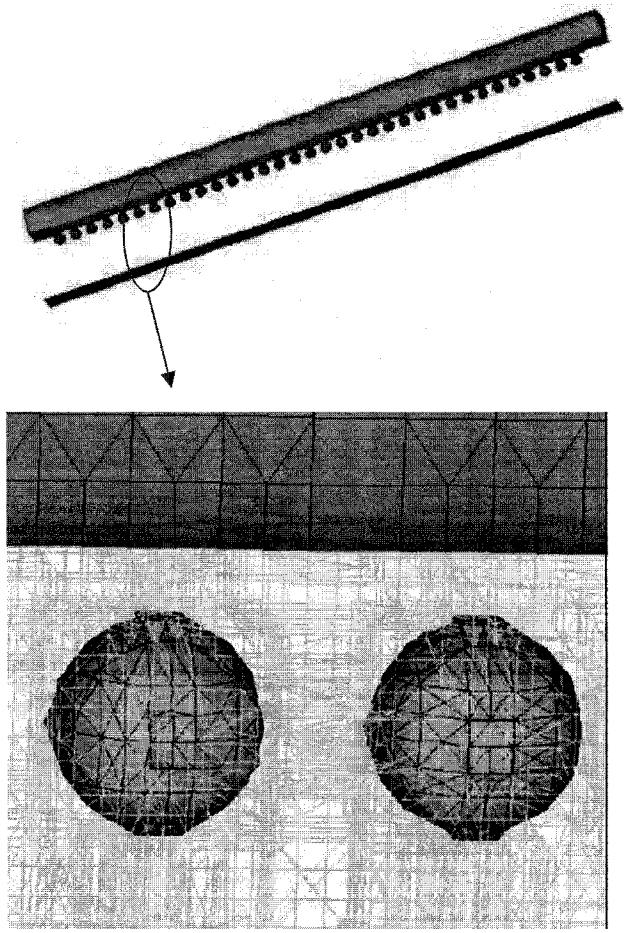


Figure 6-4 Simplified structure model (upper) and 3D mesh (bottom) of the OFET memory device.

In Figure 6-4, the random distributed gold nanoparticles are treated as one row of spherical gold nanodots (Dia. =20 nm) with 10 nm spacing. The channel length is 1.0 μm and the channel width is 30 nm. Other parameters are the same as in the 2D device. Figure 6-5 shows the normalized Q-t characteristics of the 3D device, together with the 2D

simulation result. Two Q-t curves are similar. However, the charging processes do not saturate in 3D simulation after 0.1 second charging and the final charge amount is two orders of magnitude less than the 2D result.

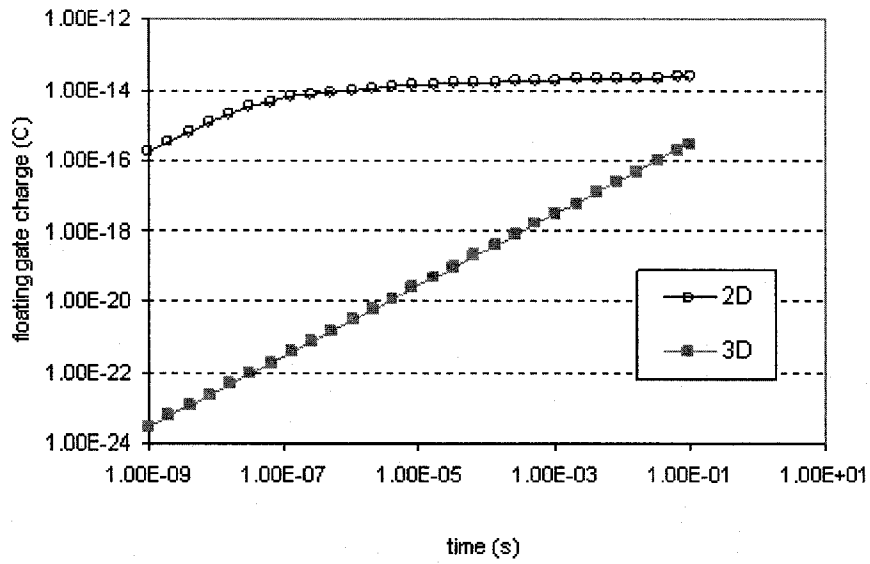


Figure 6-5 Comparison between 3D simulation and 2D simulation of floating gate charging. The thickness of control oxide and tunnel barrier are 100 nm and 10 nm, respectively.

Based on the above results, it seems that the 2D simulation gives overestimated results for the charge storage. But it still qualitatively agrees with the 3D simulation. Hence, considering the much less computation time, 2D simulation is an attractive approach for virtual device fabrication.

6.3 Fabrication of Metal Nanodot OFET Memory

6.3.1 Preparation of Gold Nanoparticles

Gold nanoparticles with the size of about 16 nm are prepared by citrate reduction method [129]. It is a 2.5 x 10^{-4} M gold colloid. First, make a stock solution of ~5.0 x 10^{-3} M $HAuCl_4$ in deionized (DI) water and store it in dark. Then take 1 ml that solution and

add it to another 18 ml DI water. Second, make a solution of 0.5% sodium citrate (0.25g in 50 ml of H_2O). Third, heat the 19 ml solution of $HAuCl_4$ to tender boiling and add 1 ml of 0.5% sodium citrate solution, as soon as boiling commences. Continue heating (~15 min) until color change is evident (pale purple). After that, stop heating and continue to stir until it has cooled to room temperature. Finally, top the solution with DI water up to 20 ml to compensate for evaporation loss due to boiling. UV-Visible absorption spectrum of the aqueous solution is shown in Figure 6-6. The plasmon absorption peak (~527 nm) indicates the existence of Au nanoparticles [130].

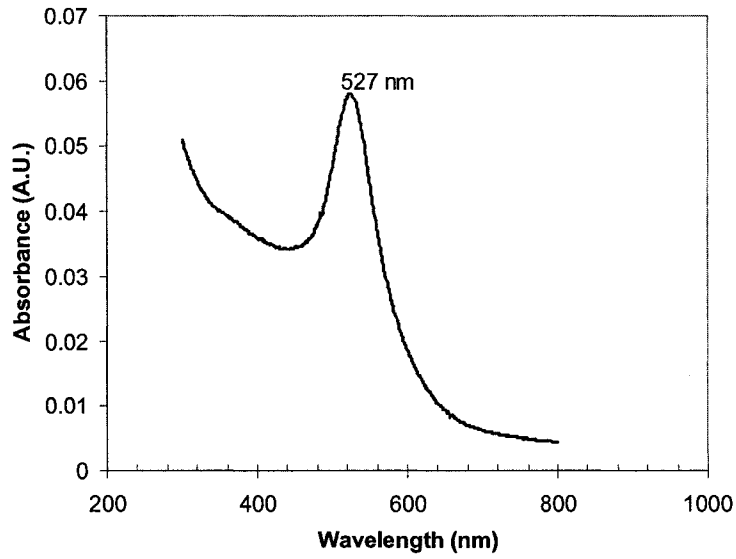


Figure 6-6 UV-VIS absorption of gold nanoparticles in water.

6.3.2 Device Fabrication

The fabrication procedure of our OFET memory cell is shown in Figure 6-7. We start with a heavily-doped N-type silicon (n^+-Si) substrate with thermally-grown oxide layer (~100 nm). N^+-Si serves as the gate while the oxide layer as the gate dielectric. The substrate is cleaned by sonicating in acetone for 10 min and then in isopropyl alcohol for another 10 min followed by multiple rinses with deionized (DI) water.

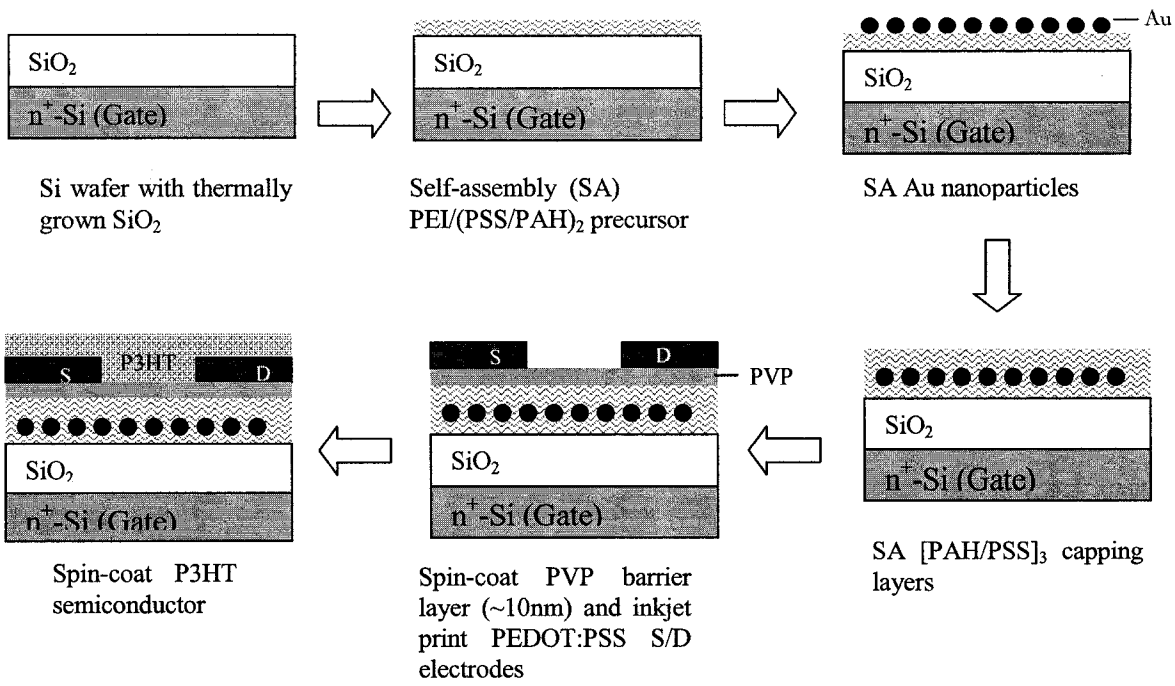


Figure 6-7 Schematic illustration of the fabrication process flow of OFET memory.

Gold nanoparticles are deposited on the oxide surface by electrostatic layer-by-layer self-assembly using polyions as the binding agents. Driven by electrostatic force between Au particles and polyions, one monolayer or even a superlattice of Au nanoparticles can be self-assembled on a "positively" charged surface. The polyions we used are poly(ethyleneimine) (PEI, MW = 70,000), poly(styrene sulfonate) (PSS, MW=65,000), and poly(allyl amine) (PAH, MW=75,000). A PEI/$(PSS/PAH)_2$ precursor film (~5 nm thick) is deposited first to reverse the charge of oxide surface and to improve the adhesion of Au nanoparitles. The topmost PAH layer is positively charged. Then the sample is immersed in the colloidal Au solution for 60 min in order to obtain good surface coverage [130]. The Au nanoparticle film is then immobilized with another ~5 nm polyion film $(PAH/PSS)_3$. The surface morphology of the Au nanoparticle film is monitored with a Quesant Atomic Force Microscope.

A thin poly(4-vinylphenol) (PVP) layer (~10 nm thick) is spin-coated to cover the gold nanoparticles, working as the tunneling barrier between the nanoparticles and the channel. After that, PEDOT/PSS (Baytron P from H.C. Starck) source/drain electrodes are inkjet-printed over the PVP layer. Channel length and channel width are controllable via the printer's computer interface. Finally, the semiconductor polymer poly(3-hexylthiophene) (P3HT) is spun on as the channel material (~20 nm). The device is ready after drying under vacuum for 12 hours at room temperature.

6.4 Characterization of Gold Nanodot OFET Memory Devices

The AFM images of the surface of Au nanoparticle film are shown in Figure 6-8. A PAH layer is self-assembled on the Au nanoparticle layer before the AFM experiment. This polyion layer is necessary because it is difficult to obtain sharp AFM picture without the immobilizing PAH layer [130]. From the AFM images, we cannot see single discrete Au particles with diameter around 16 nm. Instead, we see pebble-like ridges with longitude of 150~200 nm and lateral size of 80~100 nm, which may be caused by the filling and bridging of PAH polyions. The height (~12 nm) of these features is slightly less than the nanoparticle size ~16 nm, which could be attributed to the cushion effect of precursor layers (~5 nm).

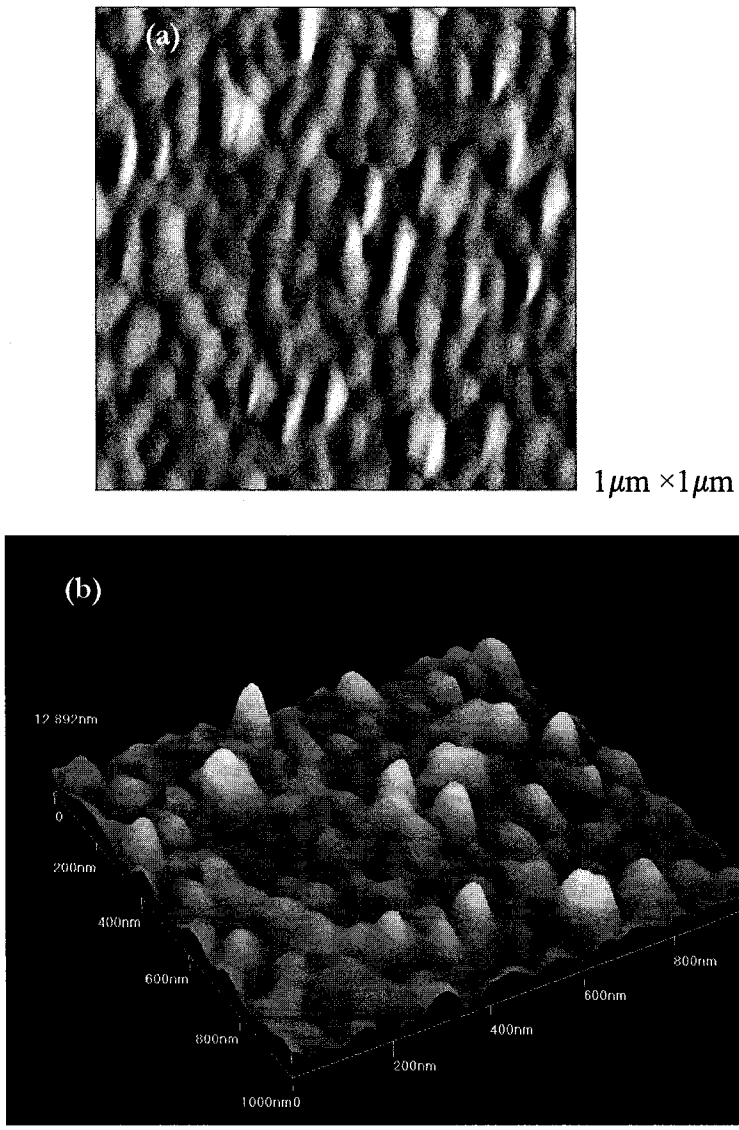


Figure 6-8 2D (a) and 3D (b) AFM images of self-assembled Au nanoparticle film capped by one PAH layer.

All devices are characterized using a Keithley system with a probe station. The I_{ds}-V_{ds} characteristics of the transistor are shown in Figure 6-9. The device features a p-channel FET with hole accumulation mode with applied negative gate voltage Vgs and hole depletion mode with increasing positive V_{gs}. I_{ds}-V_{ds} plot of the data taken by increasing V_{gs} is different from that of the data taken by decreasing V_{gs}. Data presented in Figure 6-4 are recorded when the gate voltage is applied in descending mode.

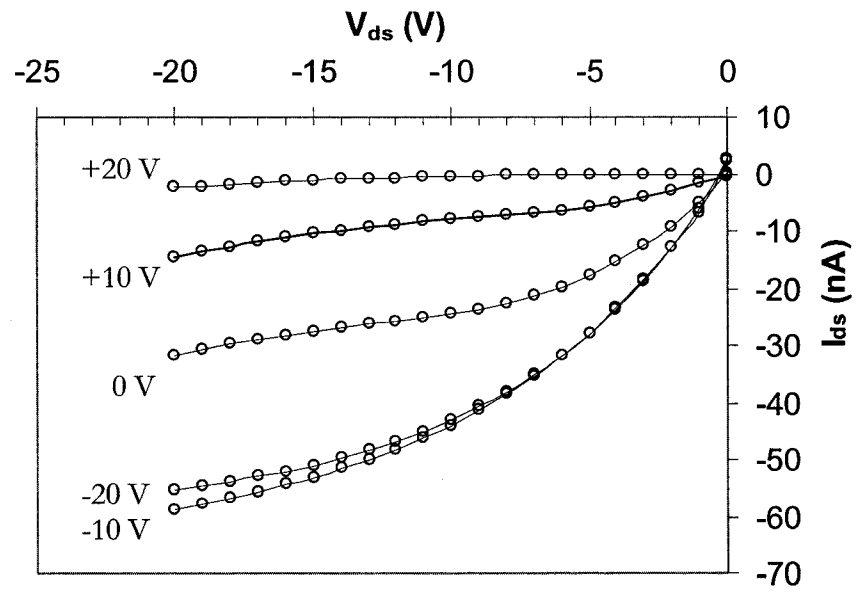


Figure 6-9 I_{ds}-V_{ds} characteristics of the organic memory transistor. V_{gs} decreases from +20 V to -20 V.

Figure 6-10 shows the transfer characteristics (I_{ds}-V_{gs}) of the transistor. Significant hysteresis loops, in anticlockwise direction, are observed when cycling voltage is applied to the gate electrode. The larger the range of V_{gs} becomes, the larger the hysteresis loops are. The on/off ratio of the drain current at V_{gs} = 0 reaches 1500. This value is close to normal P3HT-based organic transistors . We also used poly(vinyl alcohol) (PVA) and polyimide (PI) as the thin barrier insulator. Similar results were obtained.

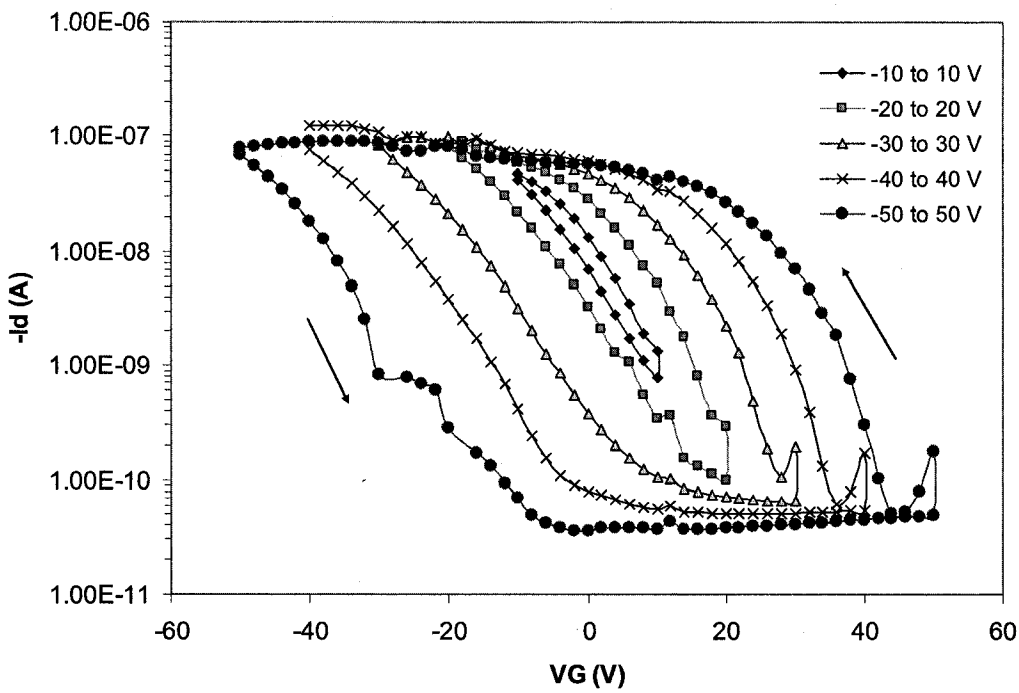


Figure 6-10 Transfer characteristics of the OFET memory device.

The effective mobility of the transistor is estimated based on the $\sqrt{I_{ds}}$ -V_{gs} curves in saturation region, where the I_{ds}-V_{gs} relation can be described as

$$I_{ds} = \frac{1}{2}\mu_{eff} C_i \frac{W}{L}(V_{gs} - V_T)^2. \qquad (6\text{-}2)$$

μ_{eff} = 5×10^{-4} $cm^2 \cdot V^{-1} \cdot s^{-1}$ is obtained. This value is one order less than the OFET we fabricated directly on SiO_2 with the same configuration. But it is in accordance with the reported mobility value in similar PVP/P3HT device configuration . The low mobility is possibly caused by the rough surface of PVP.

When the sample immersion time in the gold nanoparticle colloid is decreased from 60 min to 30 min, the on/off ratio also decreased from 1500 to 140 at V_{gs}=0 V, as shown in Figure 6-11. It seems that less gold nanoparticles are deposited in 30 minutes

than in 60 minutes. This is consistent with the report of Schmitt et al [130]. Less gold nanoparticles trap less charge. Therefore, the transistor channel is modulated at a lower extent.

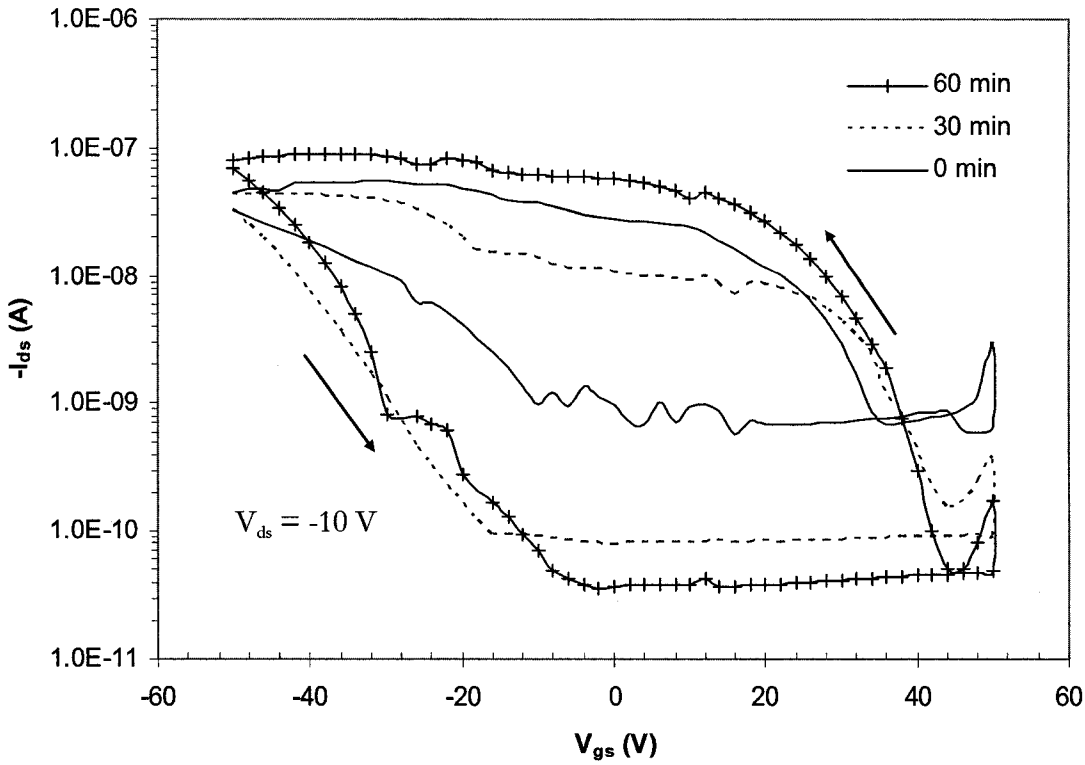


Figure 6-11 Effect of the gold nanoparticle deposition time on transfer characteristics of the polymer transistors.

The data retention time is illustrated in Figure 6-12. The ON state is obtained by biasing the gate at +40 V for 15 seconds while the OFF state at -40 V for 10 seconds. During the I_{ds}-time measurement the drain voltage V_{ds} and the gate voltage V_{gs} are both fixed at -10 V. It can be seen that the data retention time is only ~60 seconds. Such a short retention time is attributed to the poor insulating property of the PVP barrier layer and other factors that will be discussed later on.

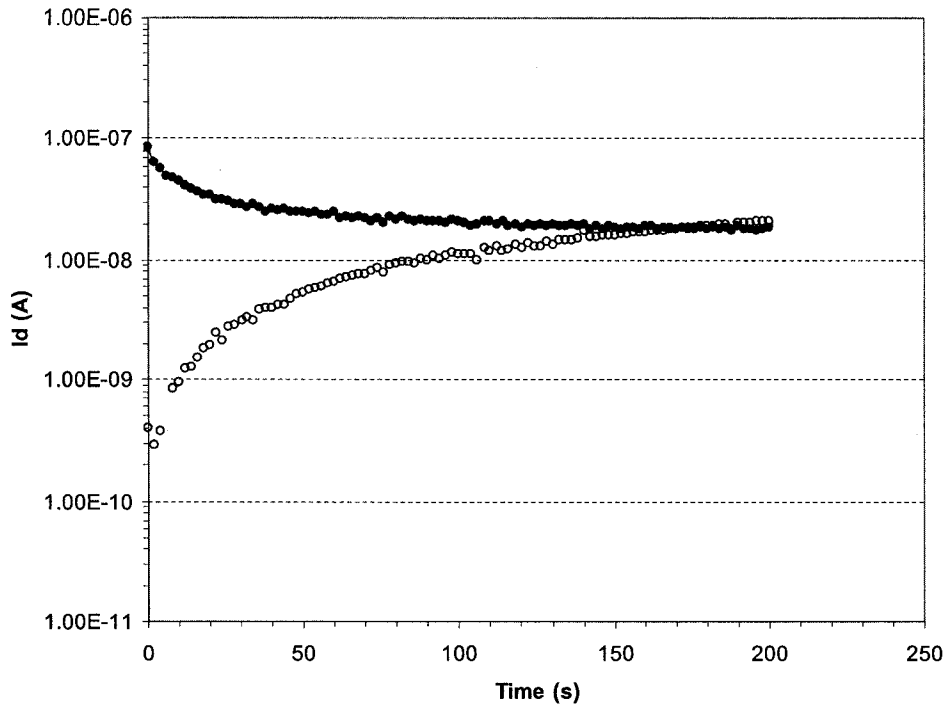


Figure 6-12 Data retention of the OFET memory.

6.5 Discussion on Factors Affecting the Device Performance

6.5.1 Effect of Traps

To confirm the charge storage effect of gold nanoparticles, a device with the same configuration, except that no gold nanoparticles are incorporated, is also fabricated and characterized. It is interesting that this device also exhibits similar hysteresis behavior (Figure 6-13) leading to two questions: 1) Does the gold nanoparticles work or not? 2) Why does the device behave this way?

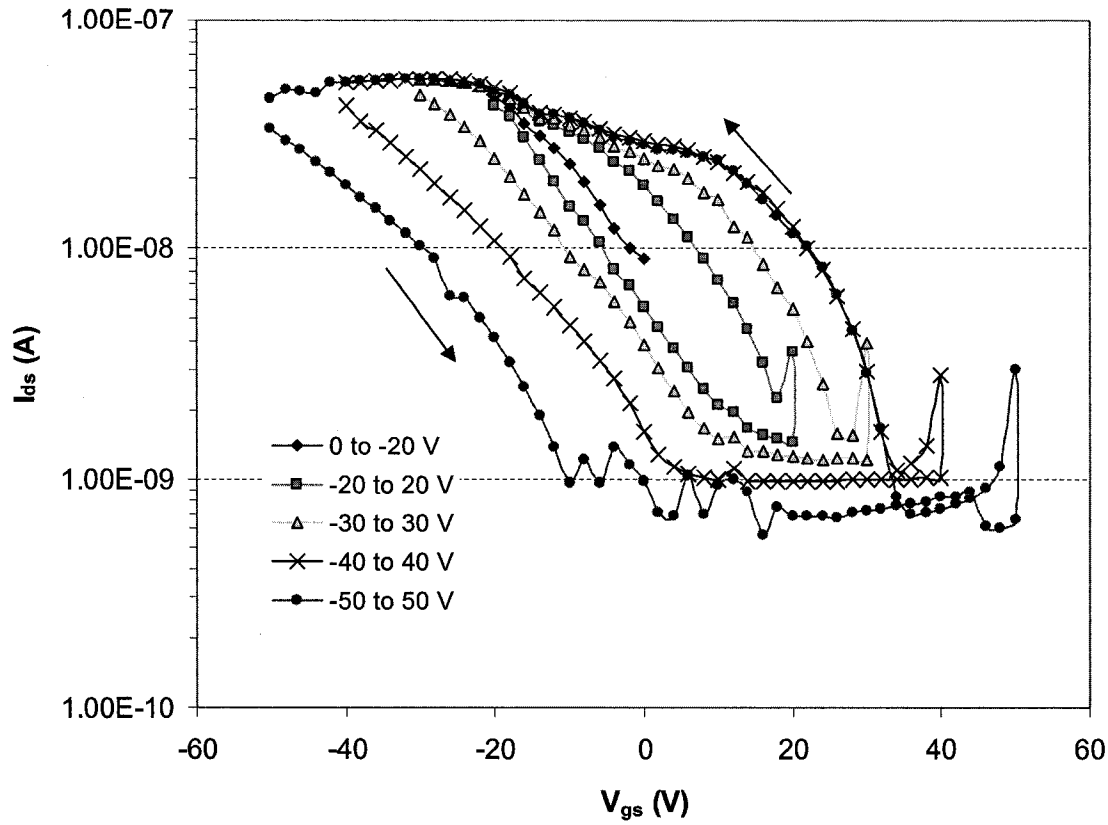


Figure 6-13 Transfer characteristics of OFET with same device configuration but without gold nanoparticles.

By comparison we find that the threshold voltage shifts of two devices are different. The threshold voltages, extracted from $\sqrt{I_{ds}}$ -V_{gs} curves, are presented in Table 6-1. Generally speaking, the V_T shift of the device with gold nanoparticles is larger than that of the device without gold nanoparticles. Hence, V_T shift contributed by gold nanoparticles could be extracted from the ΔV_T differences. From Table 6-1, we can see that the gold nanoparticles work at relatively higher program voltage. This is in agreement with the simulation results.

Table 6-1 Comparison of the V_T shift of OFETs with and without gold nanoparticles (Unit: Volts. Both devices are programmed at V_{ds} =-10 V).

Program voltage (V_{gs})	With gold nanoparticles		No gold nanoparticles		ΔV_{T1}-ΔV_{T2}
	V_{T1}	ΔV_{T1}	V_{T2}	ΔV_{T2}	
50	48	35	40	26	9
40	40	27	39	25	2
10	15	2	14	0	2
0	13	0	14	0	0
-10	10	-3	12	-2	-1
-20	2	-11	10	-4	-7
-30	-4	-17	5	-9	-8
-40	-14	-27	4	-10	-17
-50	-21	-34	-2	-16	-18

Then what should be responsible for the threshold voltage shift of the device without gold nanoparticles? The most probable reason is the charge traps, which usually exist in thin film transistors, both inorganic and organic. In our devices charge traps may exist in the organic semiconductor P3HT film, in the PVP film, at the PVP/P3HT interface and SiO_2/PVP interface.

6.5.2 Top-Contact Device Configuration

We fabricated a top-contact device by inkjet printing PEDOT:PSS on top of the semiconductor layer, as shown in the inset of Figure 6-14. The retention is significantly improved. If the charge is stored in the P3HT layer, then the above configuration change will not impart significant effects on the charge retention since PEDOT:PSS electrodes are directly contacted with P3HT channel in either case. Therefore, we can claim that the effect of traps in P3HT film is negligible here.

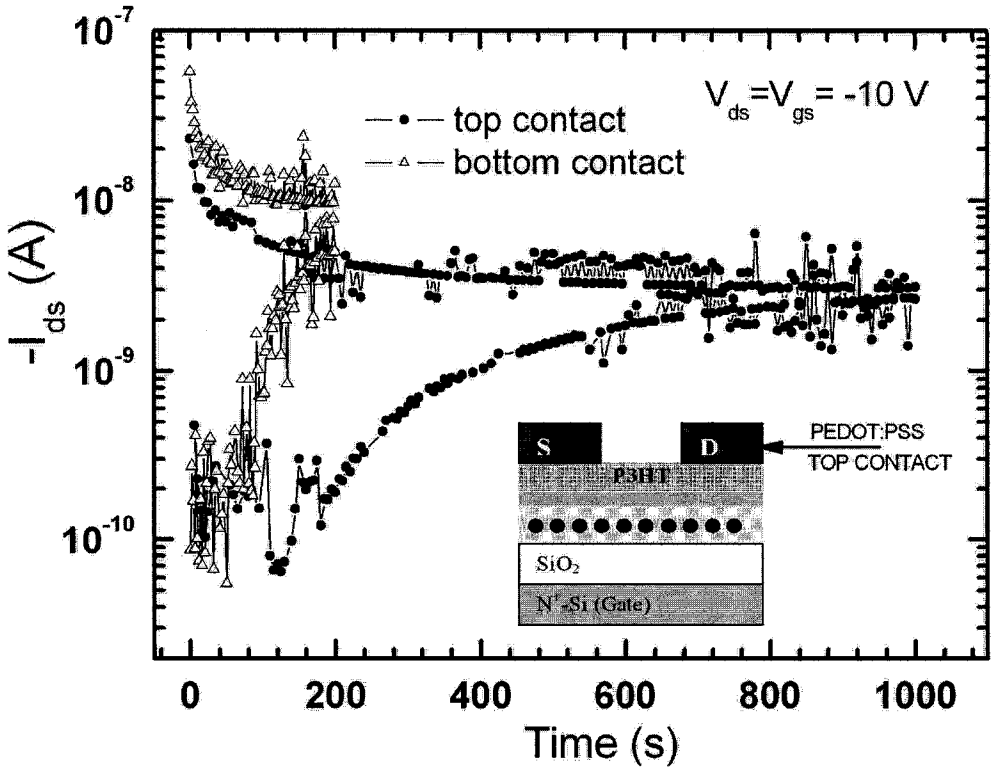


Figure 6-14 Data retention improvement using top-contact device configuration.

6.5.3 OFET with PVP-only Gate Dielectric

The effect of bulk PVP film is also studied using a PVP-only gate dielectric configuration. PVP does not play a role in the formation of hysteresis. However, the direction of loops is clockwise (Figure 6-15), in contrast to the anticlockwise loops of the devices with gold nanoparticles. Park et al. [131] also reported the clockwise loops caused by PVP gate dielectric in a pentacene TFT. On the other hand, the PVP films in our devices are very thin (~10 nm). According to Park et al [131], the hysteresis is suppressed in ultrathin PVP films. Hence, the contribution from bulk PVP film should be insignificant.

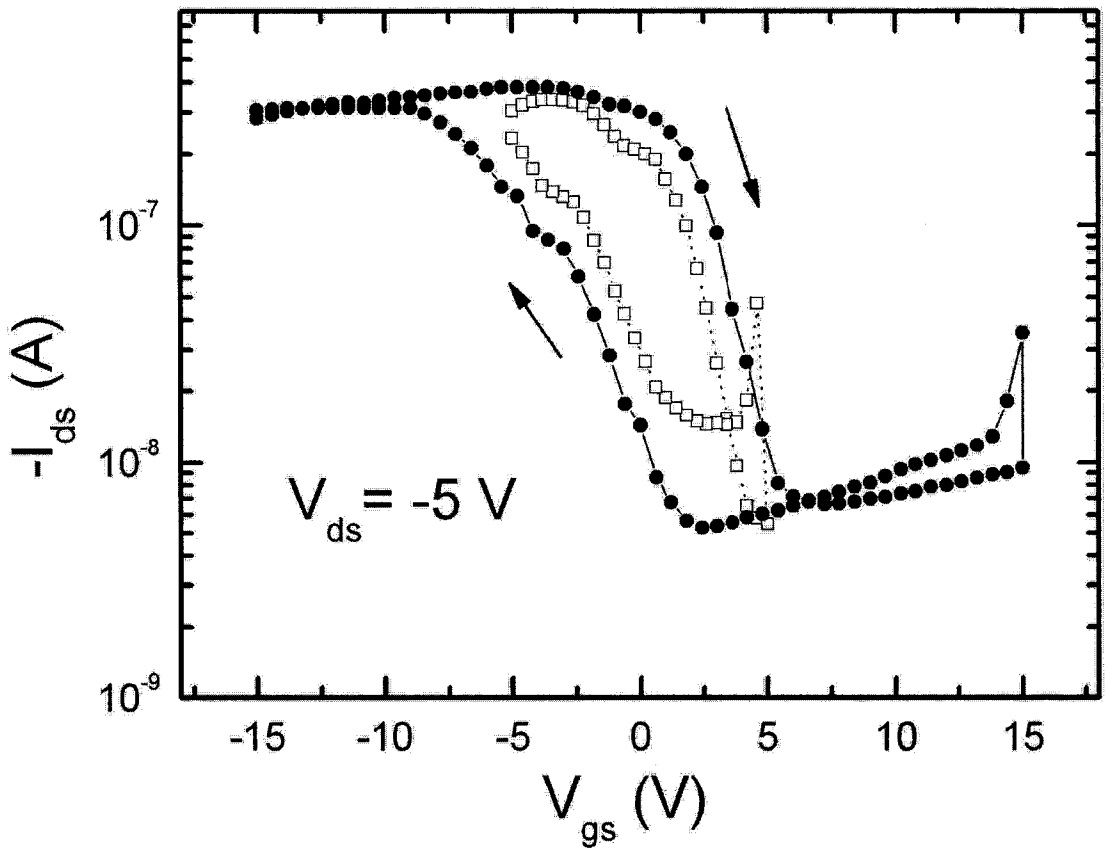


Figure 6-15 I_{ds}-V_{gs} characteristics of P3HT TFT with PVP-only gate dielectric. The hysteresis loops are clockwise.

Based on the above discussion, it seems that the traps at the PVP/P3HT interface and/or SiO_2/PVP interface play an important part in the hysteresis formation. Chua et al. [127] demonstrated that the surface OH groups are electron traps in chemistry nature. Since both SiO_2 surface and PVP surface are abundant of OH groups, it is reasonable that the electron traps exists at both SiO_2/PVP interface and PVP/P3HT interface.

Let us first consider the dielectric/P3HT interface. Hysteresis loops are also evident when P3HT layer is directly deposited on the SiO_2 surface with patterned gold S/D electrodes. Here, we further disclose the effect of dielectric/P3HT interface.

6.5.4 Insulator/P3HT Interface

In this experiment, polyimide (PI) instead of PVP was used as the tunneling barrier layer for the OFET. The reason for choosing PI is its relatively lower etch rate in O_2 plasma.

Device configuration is still the same except the PI barrier layer. Before spin-coating P3HT, PI surface is briefly treated in O_2 plasma and then silanylized with octadecanyltrichlorosilane (OTS) [132] in a dry box (dew point = -35 °C) filled with N_2. As a result, the PI surface becomes hydrophobic because OH groups were consumed and replaced by OTS molecules with alkyl tails pointing out.

Figure 6-16 shows the transfer characteristics of the devices with and without OTS treatment. It can be seen that the OTS treatment suppresses the electron trapping so as to suppress the threshold voltage shift toward the positive direction. This can be attributed to the consumption of OH groups during the silanylization. A further conclusion we can draw from the above results is that the gold nanoparticles, and probably the SiO_2/PI interface as well, trap much less electrons; otherwise, the positive V_T shift should be still significant even when the PI surface is silanylized. This is in agreement with the results of Table 6-1. A probable reason is that the tunneling barrier of electrons from channel to traps is higher than that of holes.

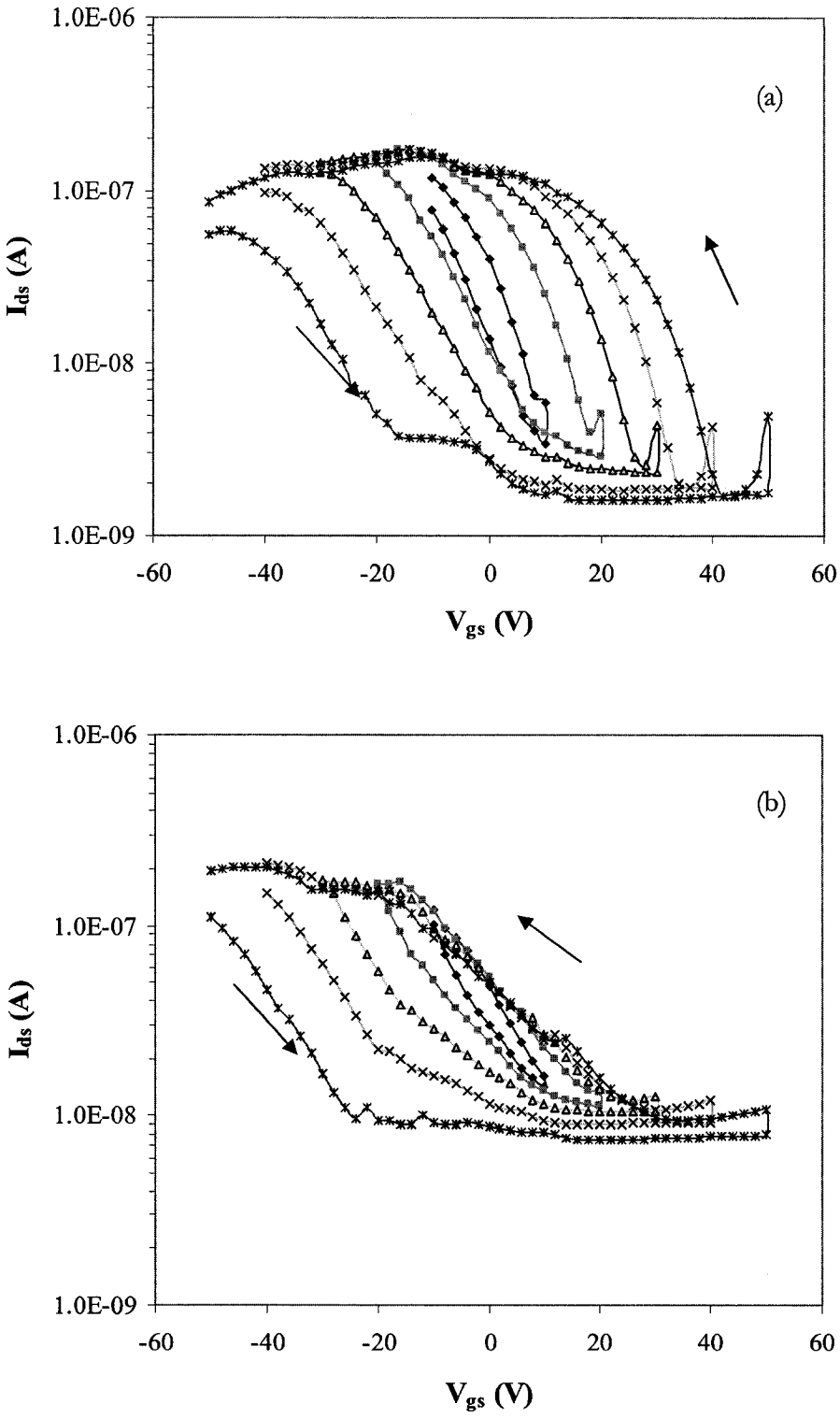


Figure 6-16 Transfer characteristics of OFETs without (a) and with (b) OTS treatment on the polyimide barrier surface.

6.5.5 Quantitative Consideration of V_T Shift

For an inorganic thin film transistor, the V_T shift is time-dependent and obeys the following equation [133, 134]:

$$\Delta V_T = B\left\{1-\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{6-3}$$

where t is the gate voltage stress time, B, τ, and β are fitting parameters that can depend on the stress voltage, stress temperature, and the device and material characteristics. We can approximately describe B using [133, 134]

$$B = V_{stress}-V_{T0} \tag{6-4}$$

where V_{T0} is the initial threshold voltage.

The experimental value of τ is usually at the level of 1000 s [61]. When the stress time $t << \tau$, for instance, $t < 15$ s in our devices, equation (6-3) can be approximated to be

$$\Delta V_T = B\left(\frac{t}{\tau}\right)^{\beta} \tag{6-5}$$

In our devices, the V_T shift versus program time ($V_{ds} = 0$) dependence is found to roughly obey Equation 6-5, as shown in Figure 6-16. Based on the $\log(\Delta V_T)$-$\log(t)$ linear fit, the B and β for positive program voltage are extracted to be 11 V and 0.29, respectively. For negative program (stress) voltage, B and β are 10 V and 0.066, respectively. It seems that the effect of negative voltage stress is less dependent on the stress time. The possible reason is that the tunneling barrier is smaller for holes than for electrons.

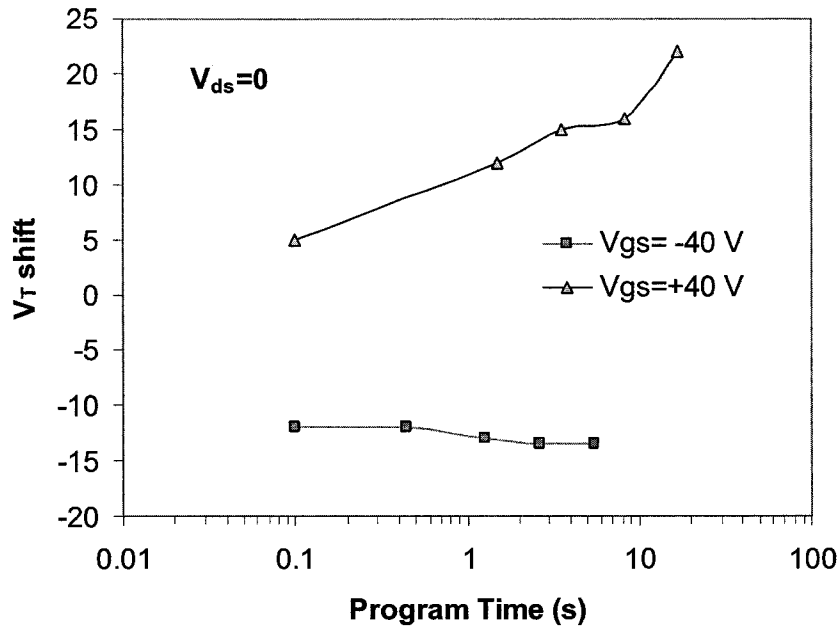


Figure 6-17 The V_T shift versus program time of the OFET memory.

6.6 Summary

In summary, gold nanoparticles were successfully integrated into the gate dielectric layer of an organic thin film transistor using electrostatic layer-by-layer self-assembly technique. The transistor exhibit significant hysteresis behavior in its current-voltage characteristics [135]. The charge storage in the gold nanoparticles was confirmed by comparing with no-gold-nanoparticle devices, although the effects of interfacial traps are also significant. The data retention time of the memory transistor is about 60 seconds. Such a short retention time is attributed to the poor insulating property of the PVP barrier layer and the fast release of the charge from interfacial charge traps. Using a thinner and better barrier insulator, e.g., Langmuir-Blogdett multilayers, should improve the device performance in terms of the data retention and mobility as well.

CHAPTER SEVEN

CONCLUSIONS AND OUTLOOK

7.1 Conclusions

An organic electrically-bistable memory device based on a spin-coated novel molecular complex thin film has been demonstrated. Sandwiched between two aluminum electrodes, the PCBM/TCNQ molecular film can switch from low-conduction state to high-conduction state upon application of an external electric field. A high current pulse can switch the device back to low conduction state. The device can remain at either state for at least five months after the external electric field is removed. This device is of potential use for low-cost write-once-read-many-times memory applications.

An improved version of the above device, a rewritable organic diode type memory device, was realized based on the ITO-PEDOT:PSS-PCBM/TCNQ-Al structure. The device exhibits a diode characteristic (low conductive) before switching to a high-conductive Poole-Frenkel regime under a positive external bias applied to ITO electrode. The on/off ratio at +1.0 V is up to 10^5. Both high-conduction and low-conduction resistances increase by a factor of two orders of magnitude after two months. But the on/off ratio hardly changes--still ~10^5. A charge storage model is proposed to explain the memory effect. Simulation results from Taurus-Medici are in qualitative agreement with the experimental results and the proposed model.

A transistor-type memory device is designed and fabricated by integrating gold nanoparticles into the gate dielectric layer of an organic thin film transistor using electrostatic layer-by-layer self-assembly technique. The device exhibit significant hysteresis behavior in its I_{ds}-V_{gs} characteristics. The charge storage in the gold nanoparticles was confirmed by comparing with no-gold-nanoparticle devices, although the effects of interfacial traps are also significant. The data retention time of the memory transistor is about 60 seconds. Such a short retention time is attributed to the poor insulating property of the PVP barrier layer and the fast release of the charge from interfacial charge traps. To the best of our knowledge, this is the first OFET memory device based on the charge storage in metal nanoparticle floating gate. The low-temperature solution-based process offers a new option to the achievement of low-cost organic transistor memory.

7.2 Suggestions for Future Work

7.2.1 Solution to the Misread Problem of Two-Terminal Memory Device

For two-terminal memory devices, there is one issue that we should pay attention to--The simple array of memory cells, which are exactly the joints of cross lines, may bring the so-called 'misread' problem. Figure 7-1 illustrates the problem. If three neighboring points (A, B, and C) in a square (or rectangular) matrix are read "1" (low impedance state), then the fourth point (D) will also read "1" even it has never been 'write-in' (should be "0"). The current can flow through the path of D-A-A'-B'-B-C-C'-D'.

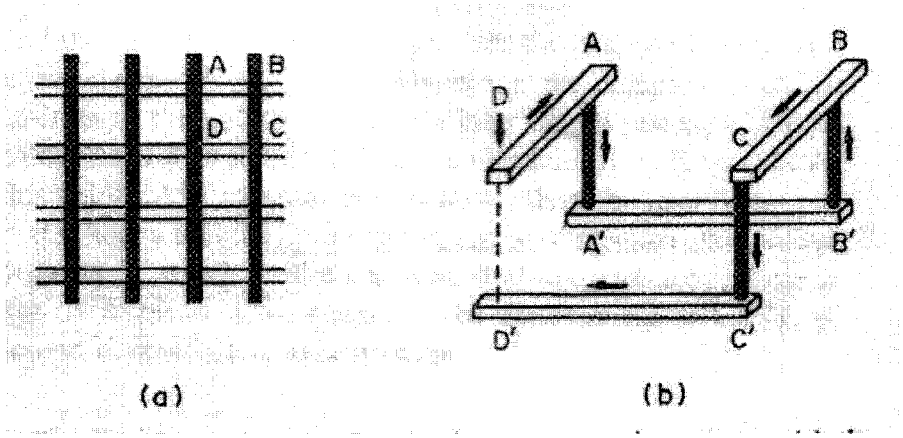


Figure 7-1 "Misread' of a matrix memory: (a) switching elements; (b) the current path.

'Misread' can be avoided by adding a diode or a transistor to each joint to block the unwanted current paths. In our diode memory devices the reverse current also dramatically increases when the device switches on. Hence, an additional diode or transistor is still needed in order to make a working memory array. The ideal solution is to make the memory diode always off in the reverse-bias regime. Another way is to make the additional diode or transistor also organic for the sake of low cost.

7.2.2 Improvement to the Performance of OFET memory

The 60 second data retention of the OFET memory is far away from practical application. Using a thinner and better tunneling barrier insulator, e.g., Langmuir-Blogdett (LB) multilayers or self-assembled monolayers (SAM), may improve the data retention. If silane SAM (e.g., OTS) is used as the tunneling barrier, the mobility and on/off ratio of P3HT channel may also be dramatically increased [100, 136].

Using pentacence may be a good way to improve the mobility of the transistor since very high mobility is reported for the OFET with PVP gate dielectric [137].

To lower the operational voltage of the OFET memory, the control gate dielectric

layer should be either very thin or of a high dielectric (high-κ) constant. For ultrathin organic gate dielectric, self-assembled monolayers of silanes were reported to be an effective approach [138-140]. For pure high-κ organic dielectrics, there are few reports yet. An alternative way is to mix the insulating polymer with high-κ nanoparticles such as TiO_2 [141], $BaTiO_3$ [142] and PCuPc [143].

7.2.3 Improvement to the Device Lifetime

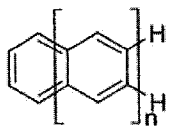
Both the diode-type and transistor-type organic memory devices are suffering from the degradation over time. The major reason for degradation is the effects of oxygen and moisture in air. Therefore, sealing and/or encapsulation is necessary for extending the device life span.

APPENDIX A

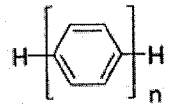
CHEMICAL STRUCTURES AND ELECTRICAL PROPERTIES OF ORGANIC SEMICONDUCTORS

(1) Chemical Structures of Organic Semiconductors

(a) Acenes and oligophenylenes:

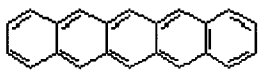


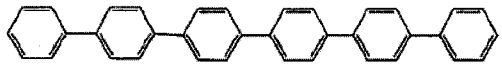
[*n*]-Acenes



Oligophenylenes

General structures





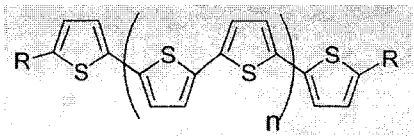
Two examples: Pentacene

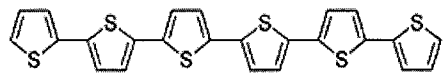
p-sexiphenyl

(b) Heterocyclic linear oligomers

Basic Elements— Heterocyclic rings:

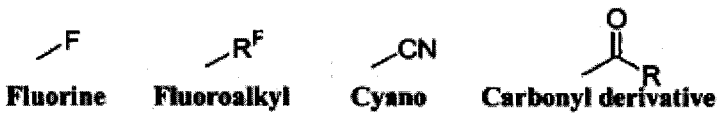
Pyridine Pyrrole Thiophene Furan Thiazole





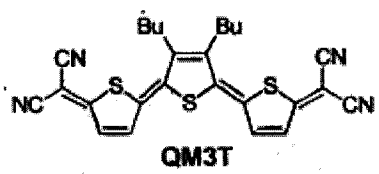
Thiophene oligomers: n=1~3, R=H or C_mH_{2m+1}

α6T

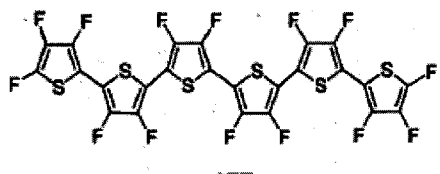


Fluorine **Fluoroalkyl** **Cyano** **Carbonyl derivative**

Electron-drawing groups

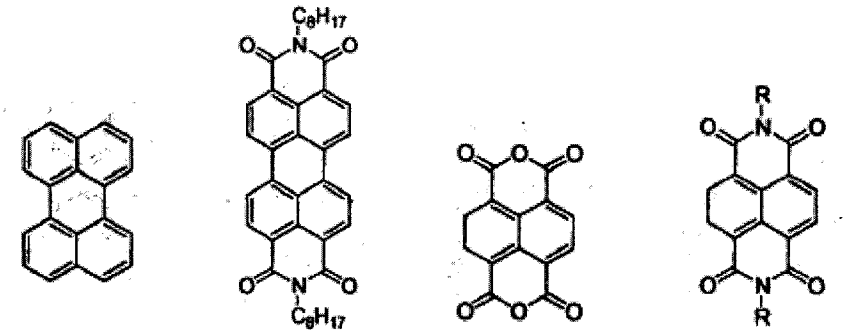


QM3T

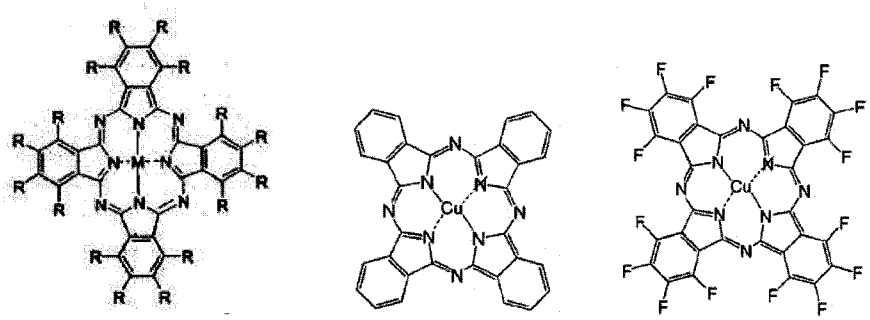


α6FT

(c) Two-dimensional fused rings



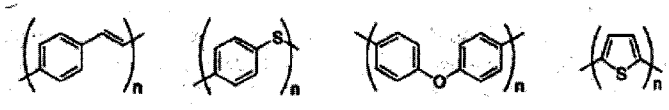
Perylene PTCDI-C8H NTCDA NTCDI (R=H or C_mH_{2m+1})

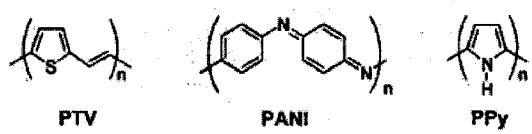


General Structure CuPc F16CuPc

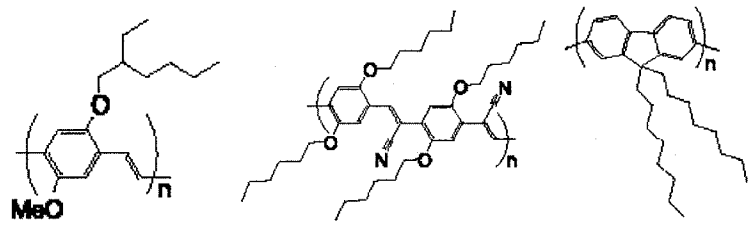
M=Cu, Zn, Fe, Co, Ni, H_2; R=H, F, Cl

(d) Polymeric semiconductors

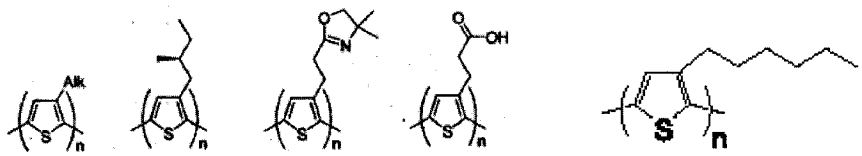




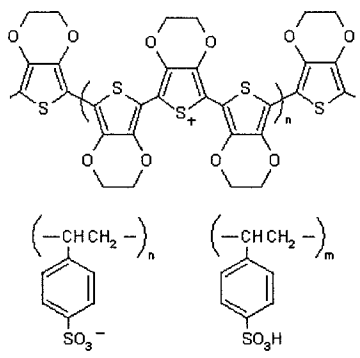
Conjugated polymer family



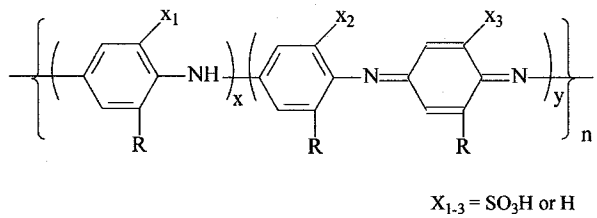
MEH-PPV CN-PPV Poly(8,8-dioctylfluorene)



Poly(3-substituted thiophene) P3HT

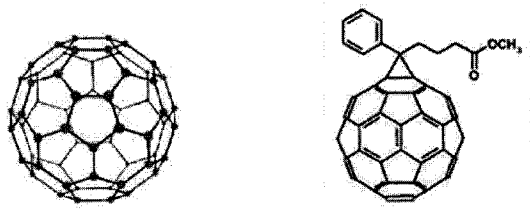


PEDOT:PSS

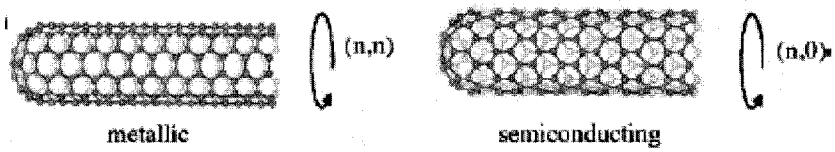


Sulfonated polyaniline

(e) Fullerenes and carbon nanotubes



C_{60} PCBM



metallic semiconducting

carbon nanotubes (Eg = 0.4~0.7 eV)

(2) Electrical Properties of Organic Semiconductors

Table A-1 Electrical properties of organic semiconductors

Name	LUMO (eV)	HOMO (eV)	μ ($cm^2 \cdot V^{-1} \cdot s^{-1}$)		ϵ_r	Film Deposit.	Ref.
			Hole	electron			
TCNQ	2.8	9.5		3×10^{-3}	3.4	s, v	[108] [121]
PCBM	3.7	6.1	0.008	0.002~ 0.01	3.9	s	[144]
PEDOT:PSS	3.5~3.6	5.1~5.2	0.1	1.7×10^{-6}	2.6	s	[49]
rr-P3HT	2.7	4.9	0.1	6×10^{-4}	3.0	s	[127]
F4TCNQ	5.24	8.34				v	[145]
Pentacene	2.3	4.9	3.0			v, s	[61]
α6T	3.5	5.1	0.002			v	
DH-α6T			0.05			v	
QM3T				0.005(v) 0.002(s)		v, s	
PTCDA	4.5	6.7					
PTCDI-C8H			0.6			v	
NTCDA	4.0	8.0					
NTCDI				0.005~ 0.16			[61]
perylene			0.02	0.017			
Alq3	2.1	5.8					
CuPc	3.5	5.2	0.02			v	[61]
ZnPc	3.34	5.28					[145]
F16CuPc		6.3		0.03		v	[61]
polyacetylene			10^{-4}				
PTP, PBP, PT, PANI			10^{-5} ~10^{-4}			s	
PPV	2.7	5.2	10^{-5} ~10^{-4}	10^{-4}		s	[127]
MEH-PPV	2.8	5.0	5×10^{-5}	3×10^{-5}		s	
Poly(8,8-dioctylfluorene)	2.4	5.7	3×10^{-4}	0.01		s	
CN-PPV	3.2	5.4		4×10^{-5}		s	
Sulfonated Poly(aniline)			0.01			s	[146]
Poly(pyrrole)		5.66	1.7				[147]
C60	2.65	6.2		0.08		v	
Carbon nanotube			1.2×10^{5}			v, s	[148]

Notes: s represents solution-process; v indicates vacuum-process.

APPENDIX B

INPUT COMMANDS FOR NANODOT

DIODE MEMORY SIMULATION

```
#heterojunction PEDT:PSS/PCBM:TCNQ structure

TaurusProcess

DefineDevice (
 name=heterojunction,
 minX=0.0, maxX=0.03,
 minY=0.0, maxY=0.15,
 x=0.0, dx=0.002, x=0.03,
 y=0.0, dy=0.005,
 y=0.1, dy=0.001, y=0.15,     )

DefineRegion (
 name="PEDT", material=silicon,
 polygon ( point (x=0,y=0.0)
        point (x=0.03,y=0.0)
        point (x=0.03,y=0.1)
        point (x=0,y=0.1)        ) )

DefineRegion (
 name="TCNQ", material=oxide,
   polygon ( point (x=0.01,y=0.1)
        point (x=0.02,y=0.1)
        point (x=0.02,y=0.11)
        point (x=0.01,y=0.11)
          hole ( polygon ( point (x=0.012,y=0.102)
                           point (x=0.018,y=0.102)
                           point (x=0.018,y=0.108)
                           point (x=0.012,y=0.108)
              ) ) ) )

# Define PCBM nanocrystal filler
DefineRegion (
          name="PCBM", material=GaAs
  polygon ( point (x=0.0,y=0.1),     point (x=0.01,y=0.1)
        point (x=0.01,y=0.15),       point (x=0.0,y=0.15)
          )
        polygon ( point (x=0.012,y=0.102),    point (x=0.018,y=0.102)
                  point (x=0.018,y=0.108),   point (x=0.012,y=0.108)    )
        polygon ( point (x=0.01,y=0.11),      point (x=0.02,y=0.11)
                  point (x=0.02,y=0.15),      point (x=0.01,y=0.15)  )
        polygon ( point (x=0.02,y=0.1),    point (x=0.03,y=0.1)
                  point (x=0.03,y=0.15),     point (x=0.02,y=0.15) )
      )

Profile (name=ptype,uniform, (value=0))
```

```
Profile (name=ntype,uniform, (value=0))
profile (name=ptype, region=PEDT, uniform,(value=1e17))
profile (name=ntype, region=PCBM, uniform,(value=1e16))
profile (name=ntype, region=TCNQ, uniform,(value=1e16))

#define contacts
#define anode contact on the top
DefineContact (
 name=anode,
 polygon ( point (x=0,y=-0.005),    point (x=0.03,y=-0.005)
           point (x=0.03,y=0.0),          point (x=0,y=0.0)
       )   )

 Regrid (
  InAbox (
     polygon (
      point (x=0.0,y=0.1),     point (x=0.03,y=0.1)
      point (x=0.03,y=0.11),       point (x=0.0,y=0.11)
         )    )
   meshspacing=0.001
   criterion(allinterfaces)
    )

#define cathode contact at the bottom
DefineContact (
 name=cathode,
 polygon ( point (x=0,y=0.150),      point (x=0.03,y=0.150)
       point (x=0.03,y=0.155),       point (x=0,y=0.155)
      )
          )
#define floating contact on the bottom
DefineContact (
 name=flt,
 polygon ( point (x=0.011,y=0.101),    point (x=0.019,y=0.101)
       point (x=0.019,y=0.109),      point (x=0.011,y=0.109)
      )
          )
save (meshfile=hetero-stru.tdf)

#### Device Simulation Input File: hetero_sim2.pdm ####

Taurus
DefineDevice (meshFile=hetero-stru.tdf)
Include (hetero_physics.pdm)

Contact (name=anode, type=Schottky, workfunction=4.8, barrierlowering=true) #ITO
```

```
Contact (name=cathode, type=Schottky, workfunction=4.28, barrierlowering=true) #Al
Contact (name=flt, type=floating)

Voltage (electrode=anode   value=0)
Voltage (electrode=cathode value=0)
voltage (electrode=flt, value=0)

Symbolic (carriers=0)
Numerics (iterations=100)
Solve {}

Symbolic (carriers=2)
Numerics (iterations=100)
Solve {}

#charging the floating gate
#charge (electrode=flt, value=-2.5e-17)

#Symbolic (carriers=2)
#Numerics (iterations=100)
#Solve {}

Save (
 meshFile=hetero_simul_0.tdf
 Add (
  ConductionBand ValenceBand
  ElectronQuasiFermiEnergy HoleQuasiFermiEnergy
  Recombination DirectRecombination
 )
)

Ramp (
 logFile=hetero_iv_hi.data,
 Voltage ( electrode=anode startValue=0.0 endValue=2.6 nSteps=52)
    )

Save (
 meshFile=hetero_simul_2.tdf
 Add (
  ConductionBand ValenceBand
  ElectronQuasiFermiEnergy HoleQuasiFermiEnergy
  Recombination DirectRecombination
 )
)
```

APPENDIX C

INPUT COMMANDS FOR GOLD NANODOT TRANSISTOR MEMORY SIMULATION

```
### define the device structure ###

TaurusProcess

DefineDevice (
 name=NCmemory,
 minX=0.0, maxX=1.10,
 minZ=0.0, maxZ=0.04,
 minY=-0.090, maxY=0.09, )
 Refinements (    Regrid (meshspacing=0.050 )
                  Regrid (meshspacing=0.010, miny=-0.04, maxy=-0.01 )
)

#define P3HT top layer
DefineRegion ( name="P3HT", material=silicon,
 brick (
        Point (x=0.0, z=0.00, y=-0.04) , Point (x=1.1, z=0.04, y=-0.09 )
    ) )

#define PAH/PSS tunneling layer
DefineRegion ( name="PAH_PSS", material=nitride,
 brick (
         Point (x=0.0, z=0.00, y=-0.04) ,   Point (x=1.1, z=0.04, y=-0.0301 )
    ) )

#define oxide
DefineRegion (
 name="PAH_SiO2", material=oxide,
 brick (
  Point (x=0.0, y=-0.0301, z=0.0),    Point (x=1.1, y=0.090, z=0.04),

  Hole (
    sphere ( Center (X=0.050, Z=0.020,Y=-0.02)
          Radius=0.01)

       ......
    sphere ( Center (x=1.04, Z=0.020,y=-0.02)
          Radius=0.01)
            )
    )
)

#Regrid (criterion(allinterfaces) )

#define  nanoAu fill-in
DefineRegion (
```

```
  name="Ni", material=nickel,
     sphere ( Center (X=0.05, Z=0.020,Y=-0.02)
          Radius=0.01)

     ......
     sphere ( Center (x=1.04, Z=0.020,y=-0.02)
          Radius=0.01)
       )

Regrid ( criterion(AllInterfaces))
Save ( meshFile=mem_str3d.tdf )


### Simulate the charging transient ###
### and Id-Vg characteristics ###

Taurus {device}

    DefineDevice(Name=tft, meshfile=mem_str3d.tdf)

#Define Contacts
Contact (name=gate, workfunction=4.8) #ITO
Contact (name=floatinggate, workfunction=5.10) #Au

Physics ( nickel (global (workfunction=5.10))) #Au
Physics (oxide (
         global (permittivity=6.9) #SiO2/PAH
               ))
Physics (nitride (
         global ( ElectronAffinity=0.97
               WorkFunction=5.47
               permittivity=2.22) #PAH/PSS
               ))

#.. Define P3HT properties and Turn on surface mobility
Physics (
 Silicon(
  global ( ElectronAffinity=3.3,
       BandGap(Eg300=1.9),
       Permittivity=3.0,
       ConductionDensityofStates (AtRoomTemperature=1e20),
       ValenceDensityofStates (AtRoomTemperature=1e20),)
  ElectronContinuity (
    Mobility( constant=false, mun0=6e-4,
         LowFieldMobility(SurfModelActive=True) )# from Nature 2005(3)
              )
```

```
   HoleContinuity (
      Mobility ( constant=false, mup0=5e-3,
      LowFieldMobility (SurfModelActive=True) )
            )
 )
)

# Blank state Id-Vd
#.. Bias contacts and Solve Poisson+Electron
Voltage( electrode=source, value=0.0 )
Voltage( electrode=drain, value=0.0 )
Voltage( electrode=gate, value=-10.0 )
Voltage( electrode=floatinggate, value=-0.2 )

Symbolic (carriers=2, newton, direct)
Numerics (iterations=100)
Solve {}

#.. Ramp floatinggate to 6V
#Ramp (ContactVoltage(electrode=floatinggate, startValue=-1, endValue=-3, nsteps=2) )

#.. Designate floatinggate as a floating contact and Solve for zero stored charge
Contact (name=floatinggate, type=floating)
Solve {}

Symbolic (carriers=2)
Ramp (logfile=VgId-w.data,
    Voltage (electrode=gate, startValue=12, endValue=-30, nSteps=42)
    )
Extract (Thresholdvoltage (gatecontact=gate, draincontact=drain))
Save (meshfile=FETiv1.tdf)

#.. Write operation through transient simulation
#.. Bias contacts and Solve Poisson+Electron
Voltage( electrode=source, value=0.0 )
Voltage( electrode=drain, value=-5.0 )
Voltage( electrode=gate, value=-20.0 )
Voltage( electrode=floatinggate, value=-0.2 )

Symbolic (carriers=2, newton, direct)
Numerics (iterations=100)
Solve {}

#.. Ramp floatinggate to 6V
Ramp (ContactVoltage(electrode=floatinggate, startValue=-1, endValue=-3, nsteps=2) )
```

```
#.. Designate floatinggate as a floating contact and Solve for zero stored charge
Contact (name=floatinggate, type=floating)
Solve {}

Transient (time=0.1, initialTimeStep=1e-9, logfile=wrt_trans.data)

Ramp (logfile=VgId-e.data,
    Voltage (electrode=gate, startvalue=-30, endValue=12, nSteps=42)
    )
Extract (Thresholdvoltage (gatecontact=gate, draincontact=drain))
Save (meshfile=FETiv2.tdf)
```

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